

RHIC BPM Meeting

June 26, 2008

Minutes

Attendees: Craig Dawson, Chris Degen, Justin Gullotta, Rob Michnoff, Michiko Minty, Tom Russo

1. Discussed Progress and Status

- a. Frank Naase completed configuration of the spare Altera/DSP development system PC. Justin successfully tested both systems.
- b. Calibration checks in 1006b have not been performed yet. Justin expects to complete this by the end of the week.
- c. We discussed several efforts that may be required, some which depend on the 1006b calibration check results. These include:
 - TDR'ing of all BPM signal pairs to measure end-to-end cable pair matching.
 - Recalibration of all modules using the external signal. The external signal connection options include:
 - Direct to the back of the IFE
 - To the input side of any splitters in the signal path
 - To the end of the cable in the tunnel
 - To the input of the attenuators in the tunnel
 - End-to-end system testing to confirm that each cable is connected to the expected A/B input for the expected plane.
- d. We discussed some options for tests to determine differences between the internal and external signals. Options include:
 - Compare an external signal with an internal pulse connected to the external input side of the combiner board. This will help determine if the mismatch is related to the combiner module or possibly the pulse itself.
 - Modify two combiner boards. On one (version A), short the external signal path directly to the analog circuit, and remove the internal calibration pulse signal path resistors. On the other (version B), short the internal calibration pulse signal path directly to the analog circuit, and remove the external signal path resistors. Test an external signal with version A, and the internal signal with version B. If mismatches are noted, then the problem is likely not related to the combiner board.
 - Compare an external signal connected at the standard input connectors, with the external signal connected to the combiner board input that is normally connected to the internal signal.
 - Install 0.1% resistors on the combiner board and test for improvement.
- e. Justin began documenting temperature test results.

2. Upcoming efforts

Some specific work expected to be performed over the next few weeks includes:

- a. Continue TDR cable tests. Determine the cause of the 5 o'clock Blue Vertical Q1 timing difference of 2 ns, and the cause of the 5 o'clock Blue Horizontal Q1 jumpy signal. Additional TDR'ing of DX BPM cable pairs in 1008 may also be desirable to determine the end-to-end matching. (J. Cupolo, Rob, Justin)
- b. Check calibration of IFE modules in 1006b with external signal. This will help us determine if calibration drifting has occurred, and therefore if calibration of all modules will be required. Testing must include connecting the external signal directly to the back of the IFE as well as to the input of splitters present in the signal path to determine if any differences exist. (Justin, Phil)
- c. Prepare short reports for temperature tests that have been performed, including analog signal input variations, timing trigger variations, and attenuator variations. Also prepare a short report on the feedthrough tests that have been performed. (Justin)
- d. Identify the cause of measurement differences between the internal and external signals. Install and test with 0.1% resistors on the combiner board.
- e. Determine the feasibility of recalibrating with the internal pulse when the temperature is different from the original external calibration
- f. Install and debug operational ADO in lab system. (Bob O., Justin)
- g. Store DSP code versions in clearcase. (Justin)
- h. Archive Altera gate array files in drafting area. (Justin)
- i. Continue generating list of known causes of BAD data (Rob, Todd, Michiko)
- j. Complete preparation of development system backup (Frank Naase, Justin)
- k. Plus additional work shown on the schedule

3. Longer term efforts

- a. Remap a few RHIC BPMs using the wire scanner unit, to double check the coefficients used to compute position.