

RHIC BPM Meeting

June 19, 2008

Minutes

Attendees: Chris Degen, Justin Gullotta, Rob Michnoff, Michiko Minty, Bob Olsen

1. Discussed Progress and Status

- a. Frank Naase has acquired an old PC with the required ISA slot for the backup DSP and Altera development system. Frank plans to configure the system around the first week in July.
- b. We discussed the BPM cable matching measurement results. (Test result details are provided in a separate document.)
- c. We decided to defer Justin's presentation on the BPM calibration procedure until mid-July after both Justin and Todd return from vacation/travel.
- d. Chris wrote a VI to help test the turn-by-turn timestamp problem.
- e. We discussed testing one IFE with 0.1% resistors on the combiner board, to determine if this corrects the mismatch issue between the internal and external signals.

2. Upcoming efforts

Some specific work expected to be performed over the next few weeks includes:

- a. Continue TDR cable tests. Determine the cause of the 5 o'clock Blue Vertical Q1 timing difference of 2 ns, and the cause of the 5 o'clock Blue Horizontal Q1 jumpy signal. Additional TDR'ing of DX BPM cable pairs in 1008 may also be desirable to determine the end-to-end matching. (J. Cupolo, Rob, Justin)
- b. Check calibration of IFE modules in 1006b with external signal. This will help us determine if calibration drifting has occurred, and therefore if calibration of all modules will be required. Testing must include connecting the external signal directly to the back of the IFE as well as to the input of splitters present in the signal path to determine if any differences exist. (Justin, Phil)
- c. Prepare short reports for temperature tests that have been performed, including analog signal input variations, timing trigger variations, and attenuator variations. Also prepare a short report on the feedthrough tests that have been performed. (Justin)
- d. Identify the cause of measurement differences between the internal and external signals. Install and test with 0.1% resistors on the combiner board.
- e. Determine the feasibility of recalibrating with the internal pulse when the temperature is different from the original external calibration
- f. Install and debug operational ADO in lab system. (Bob O., Justin)
- g. Store DSP code versions in clearcase. (Justin)
- h. Archive Altera gate array files in drafting area. (Justin)

- i. Continue generating list of known causes of BAD data (Rob, Todd, Michiko)
 - j. Complete preparation of development system backup (Frank Naase, Justin)
 - k. Plus additional work shown on the schedule
3. Longer term efforts
- a. Remap a few RHIC BPMs using the wire scanner unit, to double check the coefficients used to compute position.