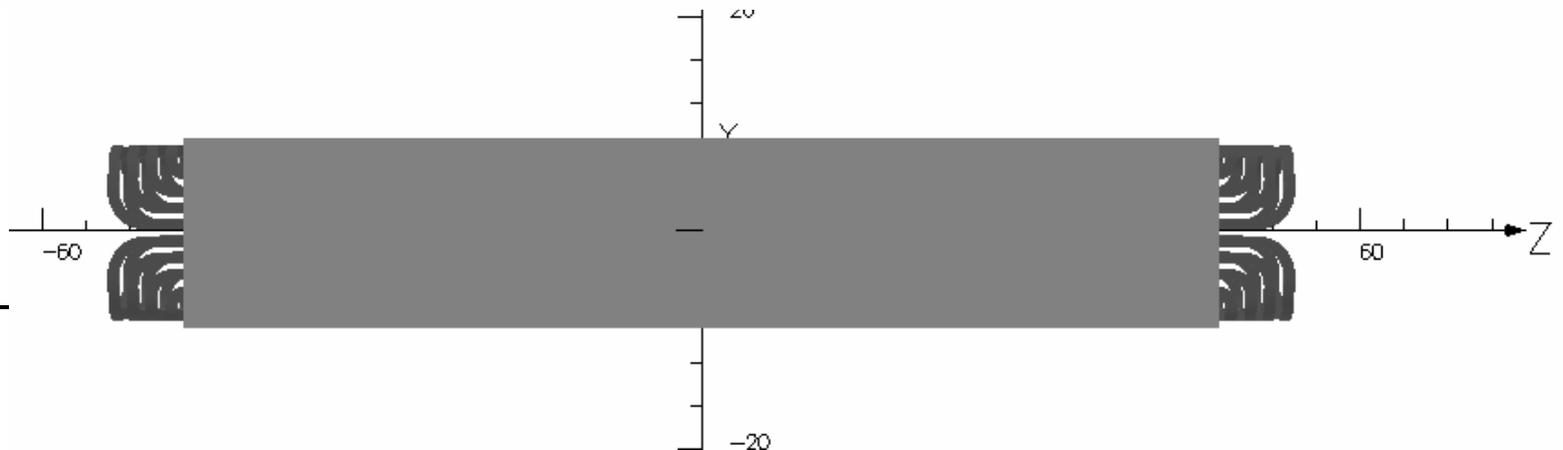
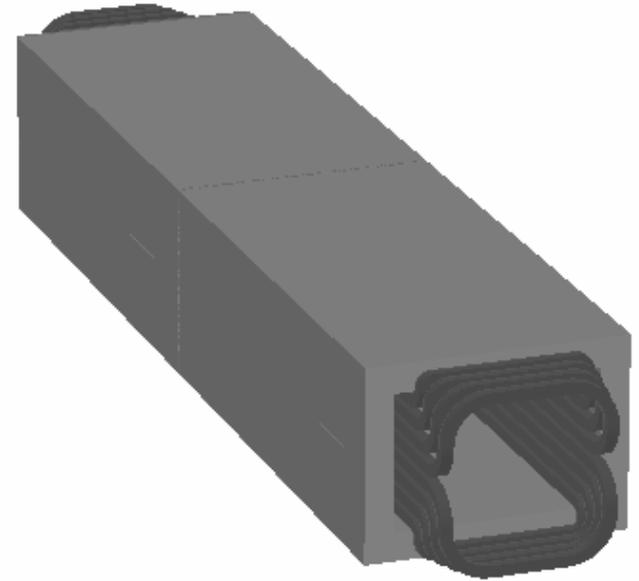
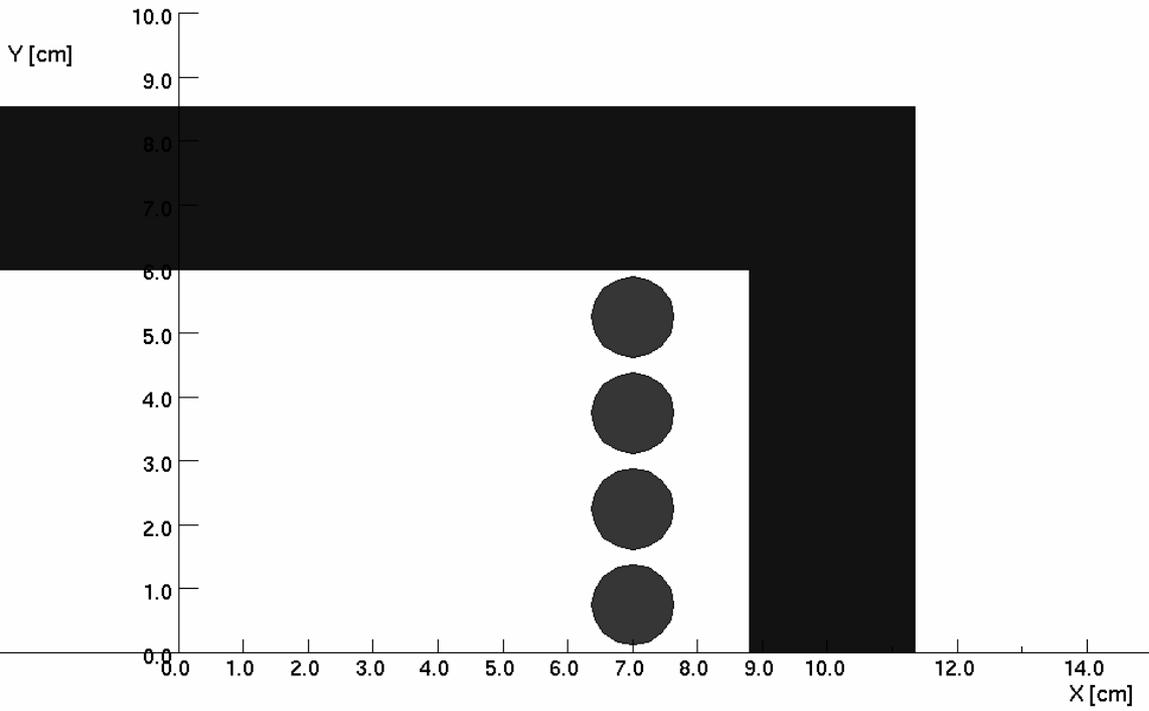


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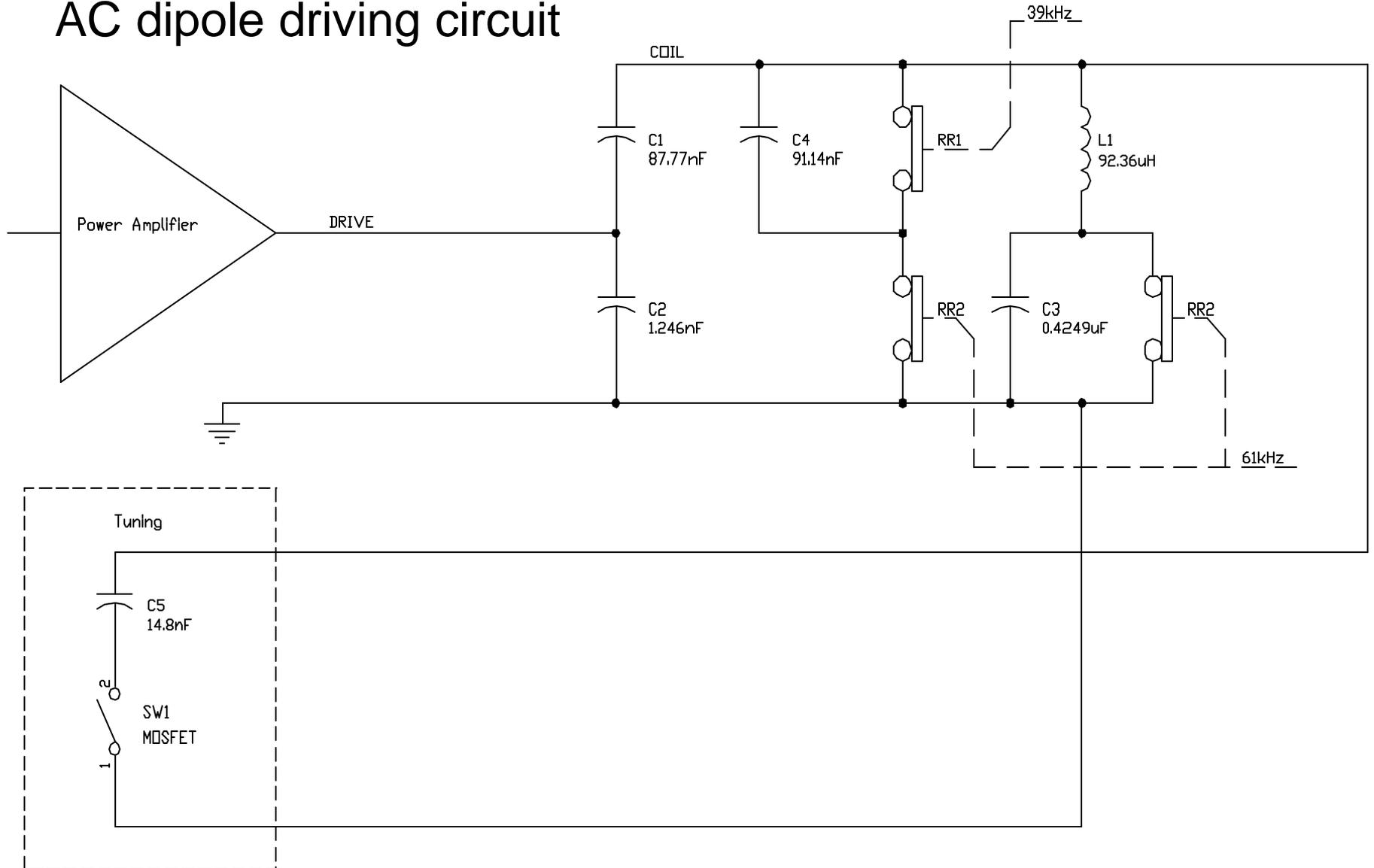
- Attendance: P. Oddo, W. Meng, C. Pai, J. Tuozzolo, J. Sandberg, T. Roser, P. Pile, Y. Makdisi, M. Bai
  - Topics
    - Magnet: see Wuzheng's and Peter's presentations
      - 8turn per magnet, Litz wire: type 2 round, 5x5x3/56/38
      - Ferrite frame: 1 inch thickness, cmd 5005
      - saddle construction, body length 92 cm. end length 7.1 cm.
      - Magnet length 99.92cm
      - $B_0=100.27$  Gauss @ 120 A
      - Inductance  $L=92.4\mu\text{H}$
      - Stored energy: 0.665Joule, dissipation
        - 39kHz: 319 w,  $Q=510$
        - 61kHz: 534 w,  $Q=534$
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# AC dipole driving circuit



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## ■ Topics

### □ cooling system: Chien-Ih's presentation

- Chien-Ih calculated heating situation due to the power dissipation of the ac dipole. His conclusion is the maximum temperature is about 80°(39kHz) and 120°(61kHz)
- Should be okay to put the non-metallic water pipes next to conductor to keep the magnet cool.

### □ Tuning circuit: Peter's presentation

- Simulation shows that the current design should provide +- 800Hz@39kHz and 2090Hz@61kHz tuning range
  - What needs to be done is to demonstrate this technique with the half meter magnet at 1kw
  - Peter is currently preparing the test setup. The most critical part is the development of the FPGA code and software driver. This is something that Peter is the only expert.
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- Joe also mentioned that he got quotes for the ceramic pipes. We all agreed that we should start to order the parts for the ac dipoles including the ceramic pipe.
  - We also discussed the potential locations for the RHIC spin flipper. Phil and Yousef will look into what need to be done for the DC spin rotators. Mei will talk to Dejan to find out which warm section will be available.
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■ Our plan is

- Goal: Install during the RHIC 2008 summer shutdown
  - Find manufacture for the ceramic pipe.
  - Purchase Litz wire and ferrite bricks
  - Need to demonstrate the dynamic tuning technique at 1kw level. For this, Peter agreed to provide a detailed work plan for the test setup at his early convenience, hopefully, by the end of January. With this plan, we can then start to work on set up the system for the high power testing while Peter continues to work on the FPGA code&software driver.
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