



CERN Beam Instrumentation DAQ Environment

US-LARP

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Rhodri Jones (CERN – AB/BDI)



Basic BDI DAQ Environment

- **VME64x chassis**
 - BDI specific backplane
 - P0 connector used for extra power supplies + timing distribution
- **PowerPC front-end controller running Lynx-OS**
 - PPC750 - speed: 400 Mhz
- **Slow timing**
 - Standard controls PMC timing mezzanine card on PowerPC
 - provides events, ms ticks & UTC timestamps
- **Fast timing**
 - BDI specific VME64x timing board
 - 40MHz bunch clock & 11kHz Frev (LVDS) distribution via P0
 - hardware triggers via P0
 - specific message information (e.g. energy intensity)
 - available via real-time task on PowerPC



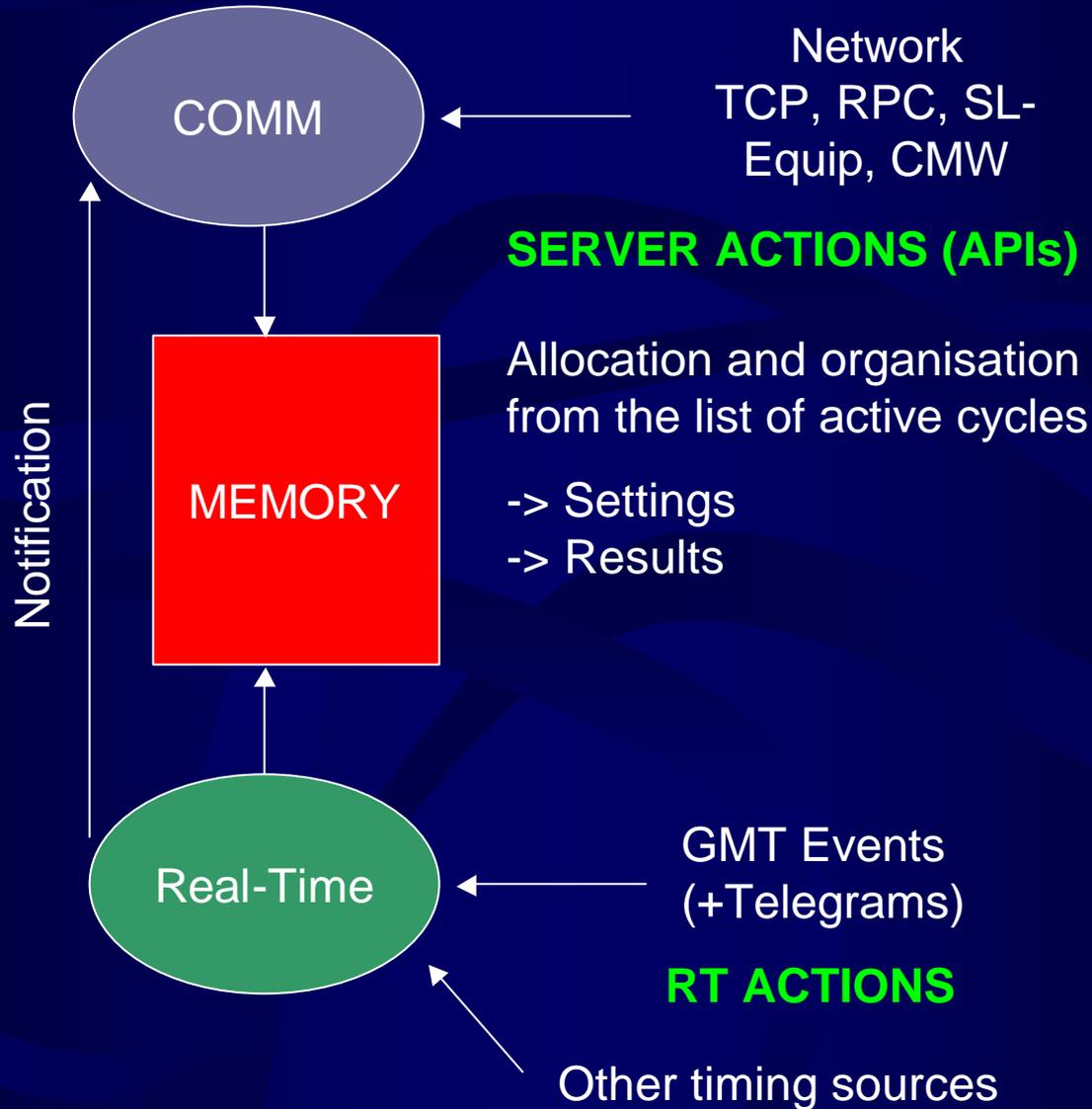
BDI low-level server development

Front-end software development is based on two parallel tasks:

1. A **communication task** that allows clients to change settings and retrieve the results from acquisitions.
 2. A **real-time task** that deals with timing (telegrams, events and BST) that triggers different real-time actions.
- The beam instrumentation software engineer's job is to use an IDE (integrated development environment) to design the APIs and the real-time actions
 - The real time actions are created empty & are coded on an instrument specific basis including any hardware access libraries

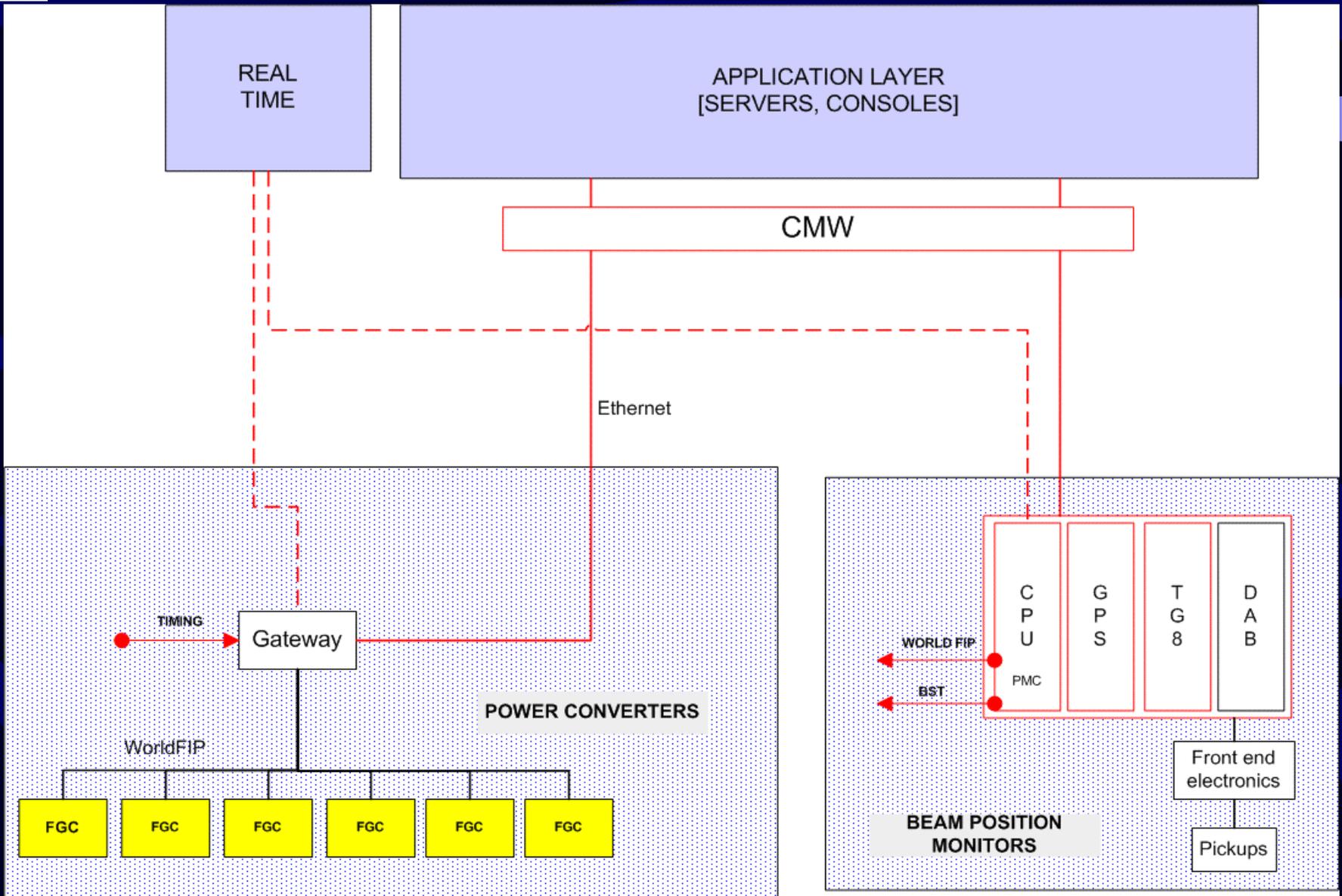


Simplified view of a BDI low-level server





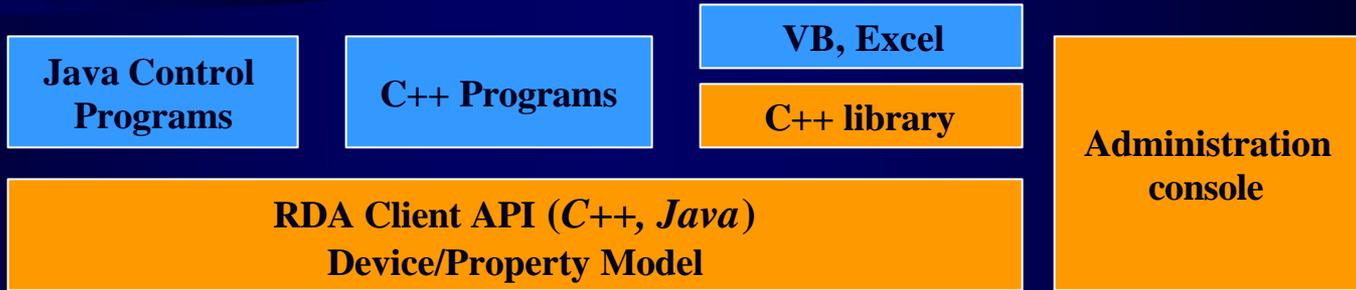
Controls System Overview



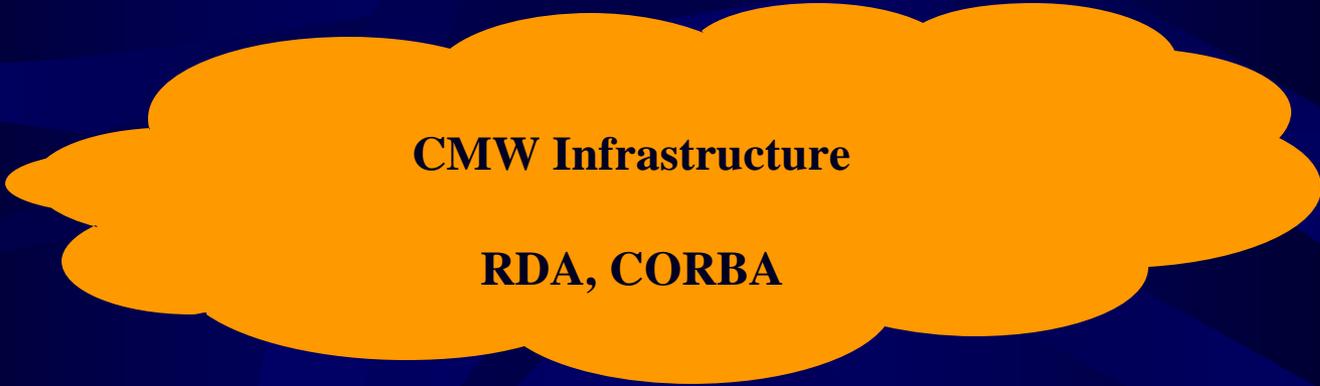


CMW Architecture

- User written
- Middleware
- Existing or off-shelf



Clients



Servers





CERN Device Access

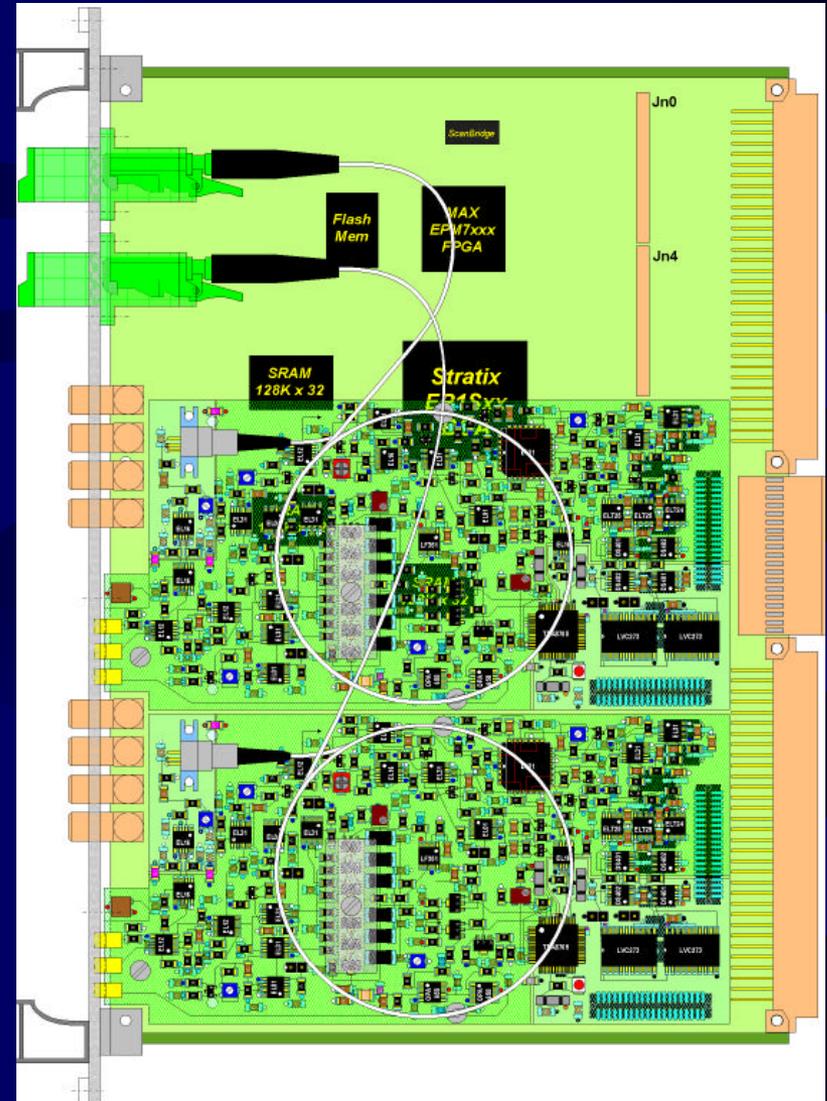
- **Common Controls Middleware**
- **Main component RDA (Remote Device Access)**
- **RDA act as a “software bus” that transparently interconnects applications and devices implemented in different languages (Java, C++,C) and running on any of the platforms used in CERN accelerator controls (Linux, HP-UX, LynxOS, Windows).**
- **Based on CORBA**
- **Narrow API (same call for all classes). The CORBA *any* type is used to transport contents of the Data objects.**
- **the standard equipment access**
- **[plus a real-time channel]**





VME64x Digital Acquisition Board (TRIUMF-DAB64x)

- 2 Mezzanines handle 12-bit 40MHz Data
- PIM Connectors extend data lines (48 & 64 bits)
- Applications so far:
 - LTI and LHC beam position systems
 - SPS, LTI and LHC fast beam intensity measurements
 - CNGS beam position system
 - LHC beam loss systems

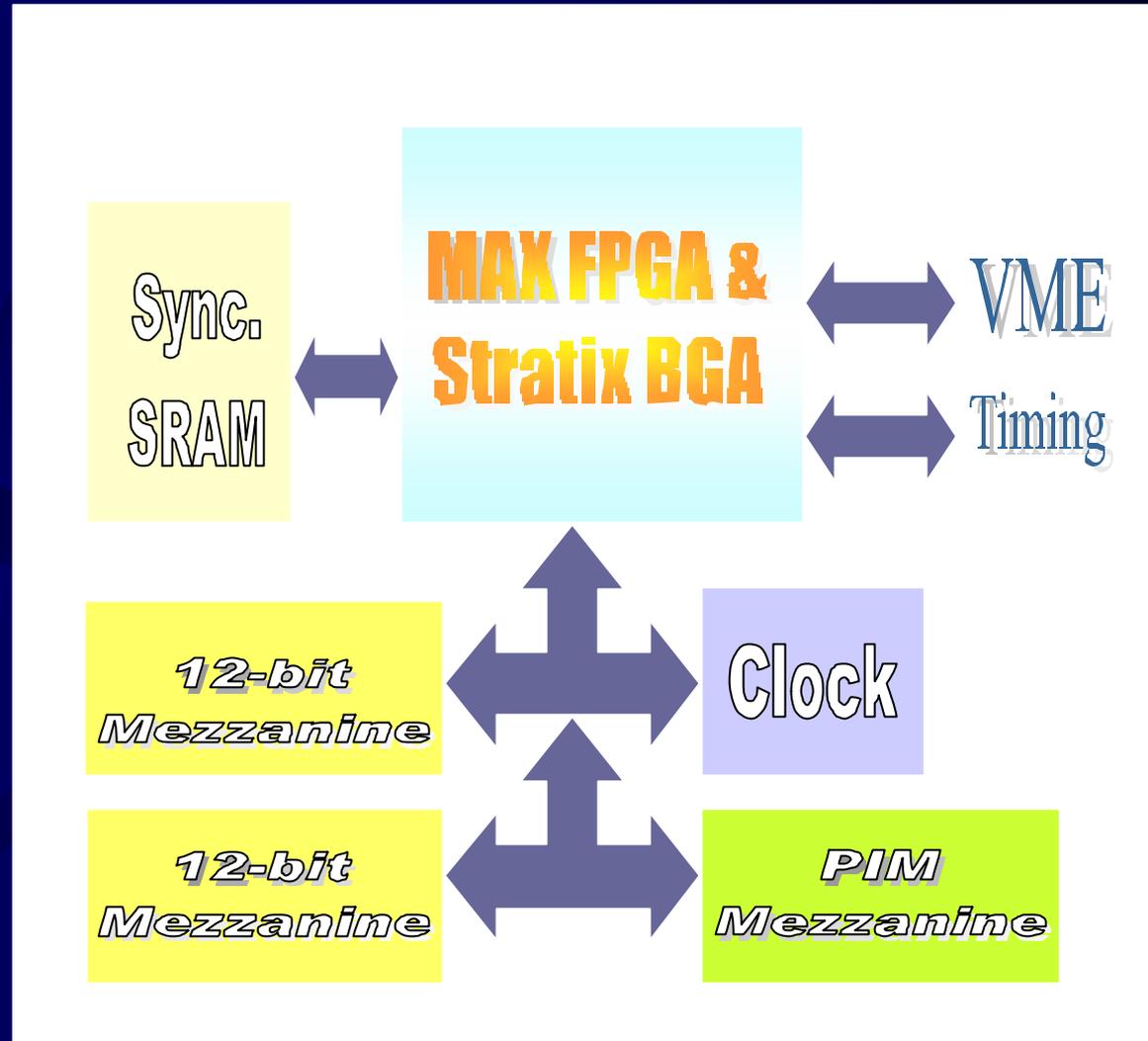




DAB64x Architecture

Main Features

- VME Access
 - D32/A32 or D64/A64
- FPGA Core
 - Altera Stratix
 - EP1S10... EP1S40F780
- Synchronous SRAM
 - 3 blocks of 128K...2M x 32/36
- 2 x 12 bit-Mezzanines
- 1 PMC I/O (PIM) Mezzanine
- Timing and Acquisition Clock management





VME64x Digital Acquisition Board (TRIUMF-DAB64x)

- The DAB64x will be used in both of the major LHC beam instrumentation systems (BLM & BPM)
 - Hardware knowledge in-house at CERN
 - Software platform for integration into CERN control system is in place
 - Guarantees long term hardware & software support
- The DAB64x architecture is very versatile
 - Altera Stratix family FPGAs allow for powerful data treatment
 - FPGA code can be changed to suit many needs
 - Can cope with 40MHz LHC data rate if required
- The DAB64x can provide a cheap, alternative data acquisition platform over expensive analysers used in specific modes of operation
 - 1 DAB64x board will cost ~1000 CHF (~\$830)



Main Devices

Cost estimates from June 2004

- **Stratix 780-Pin BGA**

→ DAB64x compatible with all variants of FPGA & memory

- **Associated Memory**

Estimated Cost

→ 3 x 128K x 32: 12 EUR

→ 3 x 1M x 32: 150 EUR

→ 3 x 2M x 36: 420 EUR

	EP1S20	EP1S30	EP1S40
Logic Elements (LEs)	18 460	32 470	41 250
M512 RAM blocks (32 x 18 bits)	194	295	384
M4K RAM blocks (128 x 36 bits)	82	171	183
M-RAM blocks (4K x 144 bits)	1	4	4
Total RAM bits	1 669 248	3 317 184	3 423 744
DSP blocks	10	12	14
Embedded multipliers (9x9-bit)	80	96	112
PLLs	6	10	12
Maximum user I/O pins	586	597	615
Estimated cost (EUR)	212	422	



The DAB64x P0 Connector

User IN/OUT

Pin	Row a	Row b	Row c	Row d	Row e	Row f
1	BLMin1	-5V2RET	-5V2RET	Capture Start	Post Mortem Start	GND
2	BLMin2	-5V2RET	-5V2RET	Auxiliary d2	Post Mortem Freeze	GND
3	BLMin3	-5V2RET	-5V2RET	Auxiliary d3	Auxiliary PM Start	GND
4	BLMin4	-5V2	-5V2	Auxiliary d4	Auxiliary PM Freeze	GND
5	BLMout1	-5V2	-5V2	Auxiliary d5	Orbit Start	GND
6	BLMout2	-5V2	-5V2	Auxiliary d6	Auxiliary e6	GND
7	BLMout3	-2VRET	-2VRET	Auxiliary d7	Auxiliary e7	GND
8	BLMout4	-2VRET	-2VRET	Auxiliary d8	Auxiliary e8	GND
9	Unused	-2V	-2V	Unused	Unused	GND
10	Unused	-2V	-2V	Unused	Unused	GND
11	Unused	Unused	Unused	Unused	Unused	GND
12	Unused	+5V	+5V	BS0	LVDS Turn clock Delay +	GND
13	Unused	+5V	+5V	BS1	LVDS Turn clock Delay -	GND
14	Unused	+5VRET	+5VRET	BS2	Unused	GND
15	Unused	+5VRET	+5VRET	BS3	Unused	GND
16	Unused	+15V	+15V	BS4	LVDS 40 MHz Clock +	GND
17	Unused	+15VRET	+15VRET	BS5	LVDS 40 MHz Clock -	GND
18	Unused	-15VRET	-15VRET	BS6	Unused	GND
19	Unused	-15V	-15V	BS7	Unused	GND

Power Supplies to Acq. Mezzanines

From BST → Cabled to Stratix FPGA



Mezzanine Connectors

POWER			DATA		
JX1			JX2		
	a	b		a	b
1	+15V	+15V	1	Turn Clk +	Turn Clk -
2	+15VRET	+15VRET	2	40MHz +	40MHz -
3	-15VRET	-15VRET	3	Delayed Trn Clk +	Delayed Trn Clk -
4	-15V	-15V	4	Delayed 40MHz +	Delayed 40MHz -
5	-5.2VRET	-5.2VRET	5	Control 0	FBCT Integrator #
6	-5.2VRET	-5.2VRET	6	Control 1	Ext Trig
7	-5.2V	-5.2V	7	Control 2	Strobe
8	-5.2V	-5.2V	8	Control 3	IR
9	-2VRET	-2VRET	9	DGnd	D11
10	-2VRET	-2VRET	10	DGnd	D10
11	-2V	-2V	11	DGnd	D9
12	-2V	-2V	12	DGnd	D8
13	+5V	+5V	13	DGnd	D7
14	+5VRET	+5VRET	14	DGnd	D6
15	Unconnected	Unconnected	15	DGnd	D5
16	Unconnected	Unconnected	16	DGnd	D4
17	DGnd	DGnd	17	DGnd	D3
18	+5VD	+5VD	18	DGnd	D2
19	DGnd	DGnd	19	DGnd	D1
20	+3.3VD	+3.3VD	20	DGnd	D0

LVDS



PIM Connectors

- The PMC I/O Module connectors extend the capability of the DAB board. They allow the connection to the Stratix of:

→48 bits on Jn0 and

→64 bits on Jn4

- Jn0 provides the main power supplies to the PMC mezzanine

Pn0/Jn0				Pn4/Jn4			
Pin	Signal Name	Signal Name	Pin	Pin	Signal Name	SignalName	Pin
1	Signal	+12V	2	1	I/O	I/O	2
3	Signal	Signal	4	3	I/O	I/O	4
5	+5V	Signal	6	5	I/O	I/O	6
7	Signal	Signal	8	7	I/O	I/O	8
9	Signal	+3.3V	10	9	I/O	I/O	10
11	Signal	Signal	12	11	I/O	I/O	12
13	GND	Signal	14	13	I/O	I/O	14
15	Signal	Signal	16	15	I/O	I/O	16
17	Signal	GND	18	17	I/O	I/O	18
19	Signal	Signal	20	19	I/O	I/O	20
21	+5V	Signal	22	21	I/O	I/O	22
23	Signal	Signal	24	23	I/O	I/O	24
25	Signal	+3.3V	26	25	I/O	I/O	26
27	Signal	Signal	28	27	I/O	I/O	28
29	GND	Signal	30	29	I/O	I/O	30
31	Signal	Signal	32	31	I/O	I/O	32
33	Signal	GND	34	33	I/O	I/O	34
35	Signal	Signal	36	35	I/O	I/O	36
37	+5V	Signal	38	37	I/O	I/O	38
39	Signal	Signal	40	39	I/O	I/O	40
41	Signal	+3.3V	42	41	I/O	I/O	42
43	Signal	Signal	44	43	I/O	I/O	44
45	GND	Signal	46	45	I/O	I/O	46
47	Signal	Signal	48	47	I/O	I/O	48
49	Signal	GND	50	49	I/O	I/O	50
51	Signal	Signal	52	51	I/O	I/O	52
53	+5V	Signal	54	53	I/O	I/O	54
55	Signal	Signal	56	55	I/O	I/O	56
57	Signal	+3.3V	58	57	I/O	I/O	58
59	Signal	Signal	60	59	I/O	I/O	60
61	-12V	Signal	62	61	I/O	I/O	62
63	Signal	Signal	64	63	I/O	I/O	64