



Tune Feedback Data Acquisition

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Outline

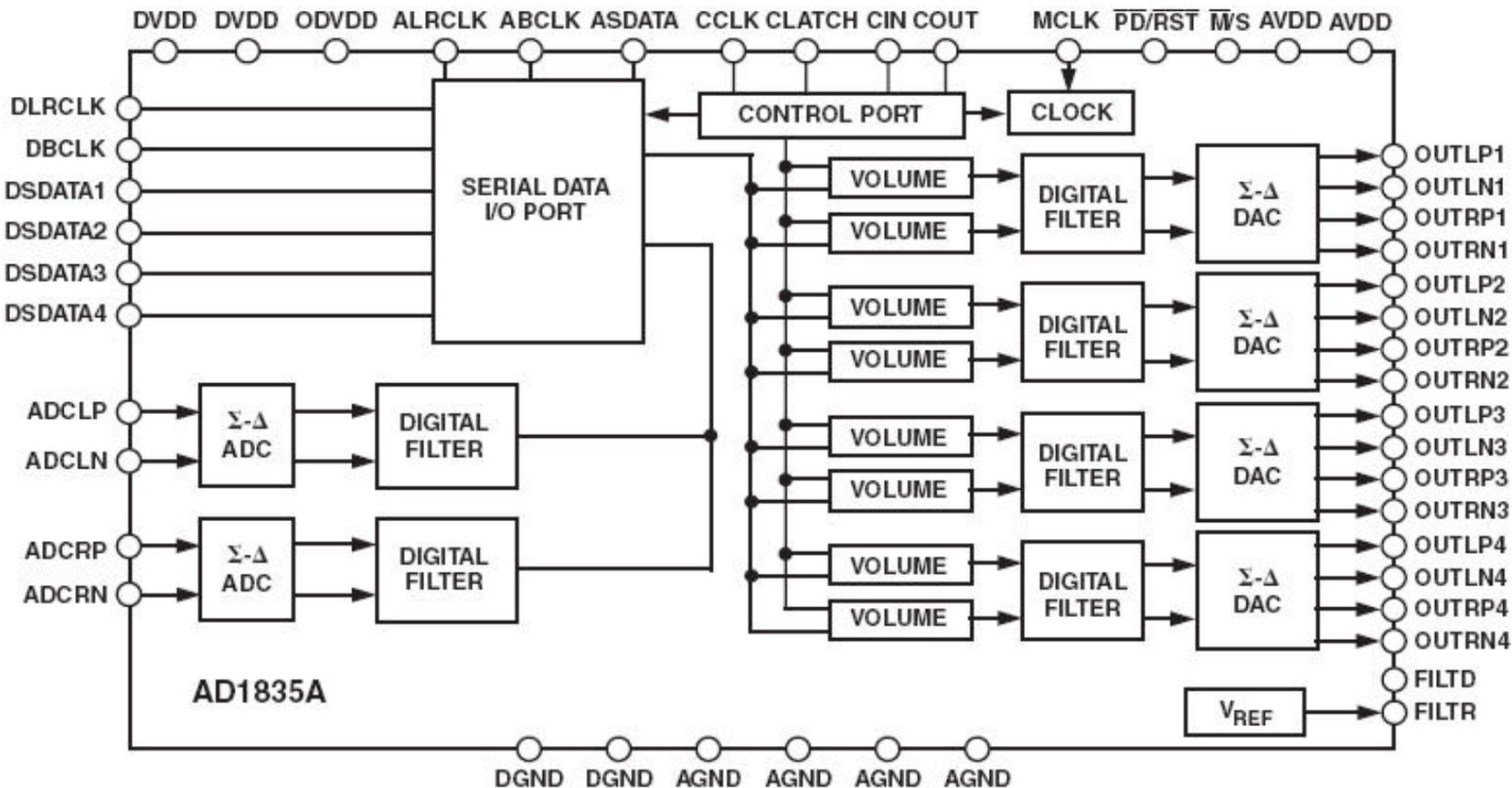


- Constraints
- Codec, DAB Board
- The RHIC Single Plane Architecture
- The LHC Single Plane Architecture
- The RHIC Controls Interface
- The LHC Controls Interface
- Boundaries
- Summary

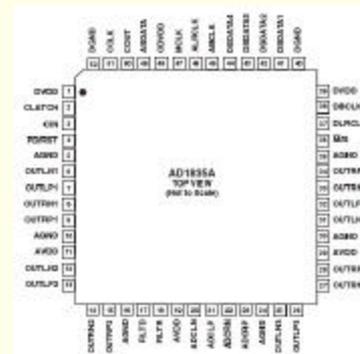
Constraints

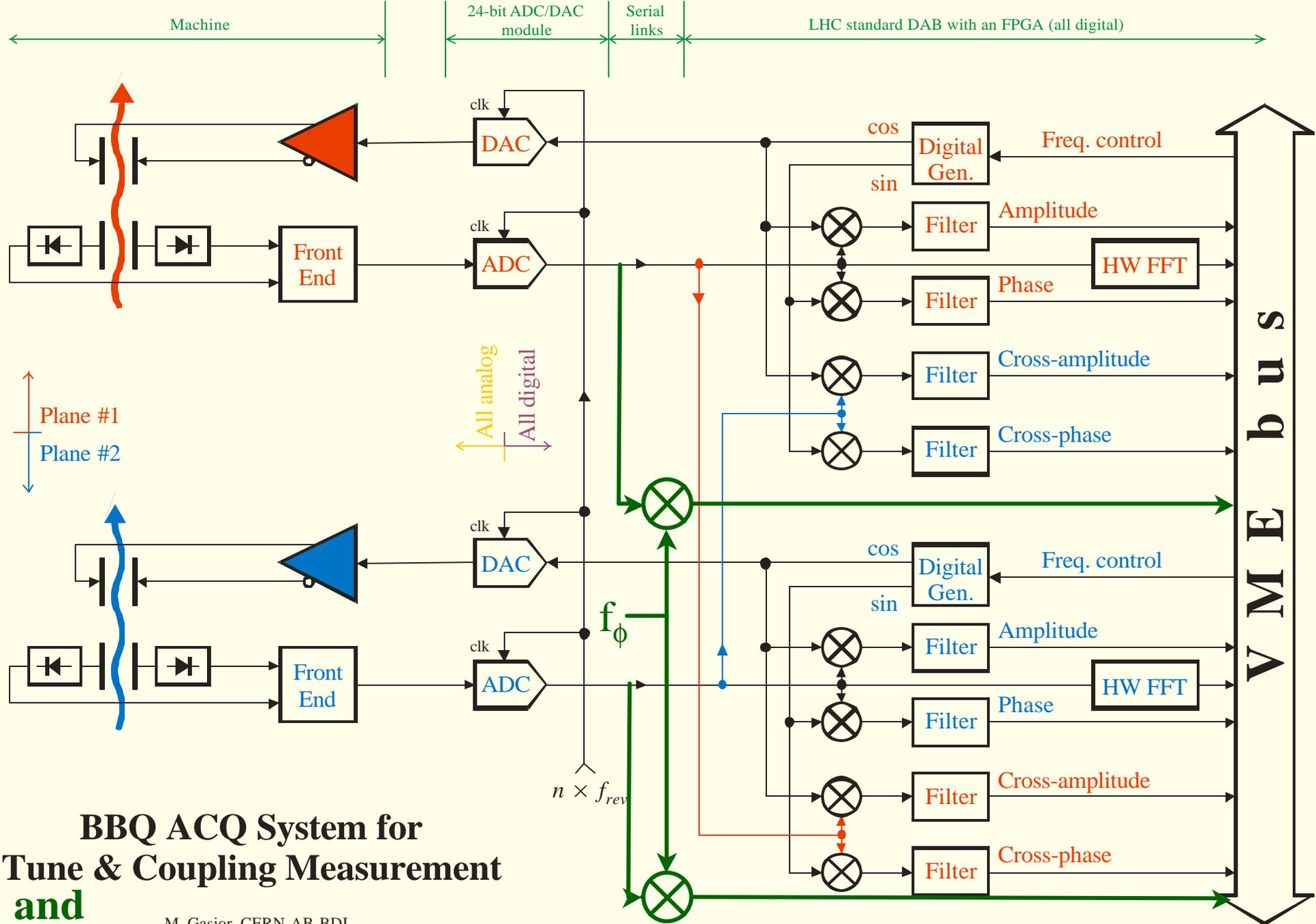


- Hardware compatibility between RHIC and LHC
 - essentially the same beams, at different frequencies
- Software compatibility between RHIC and LHC
 - common platform - VME
 - vXworks (BNL) and lynxOS (CERN)
 - LabVIEW and FESA
- Maintainability, Obsolescence,...
- Manpower - keep it simple
- Schedule

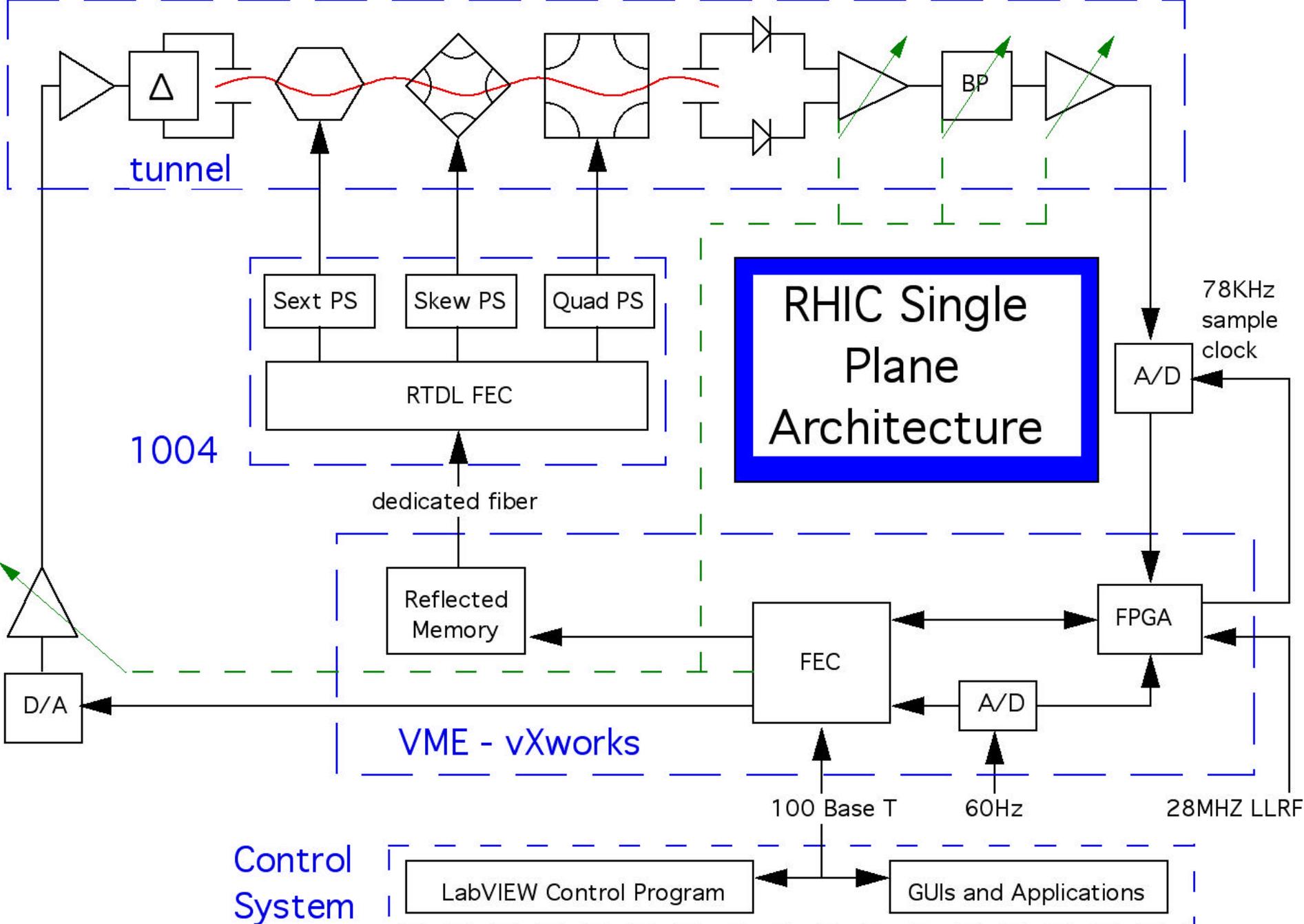


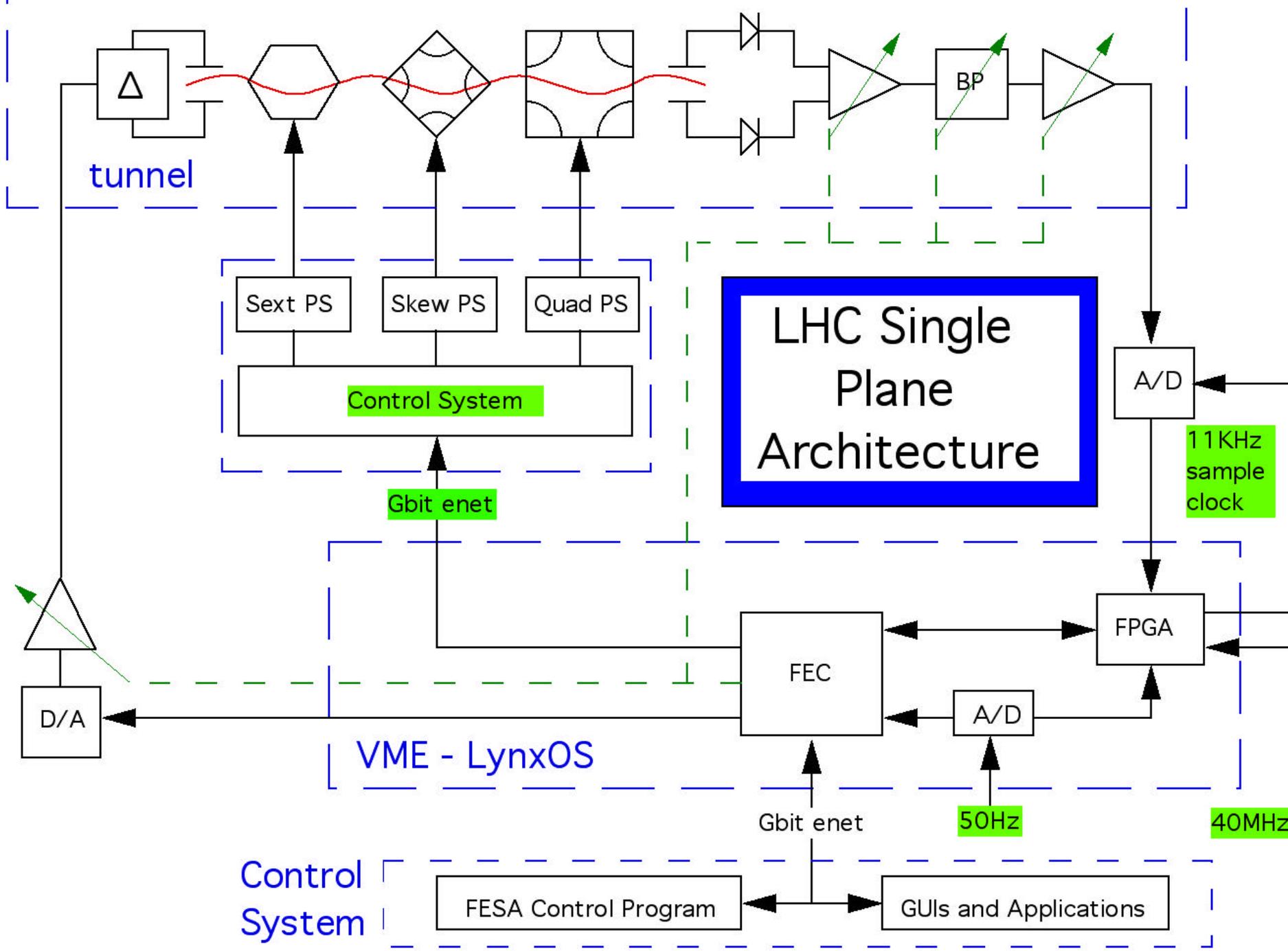
- In one chip 2 ADCs / 8 DACs, 24 bit, 96 kS/s
- SNR 105 dB (i.e. some 18 true bits)
- It can work with any sampling frequency (< 96 kS/s)
- Everything controlled through a single bus (a few serial links)
- Some digital filters already inside





BBQ ACQ System for Tune & Coupling Measurement and chrom

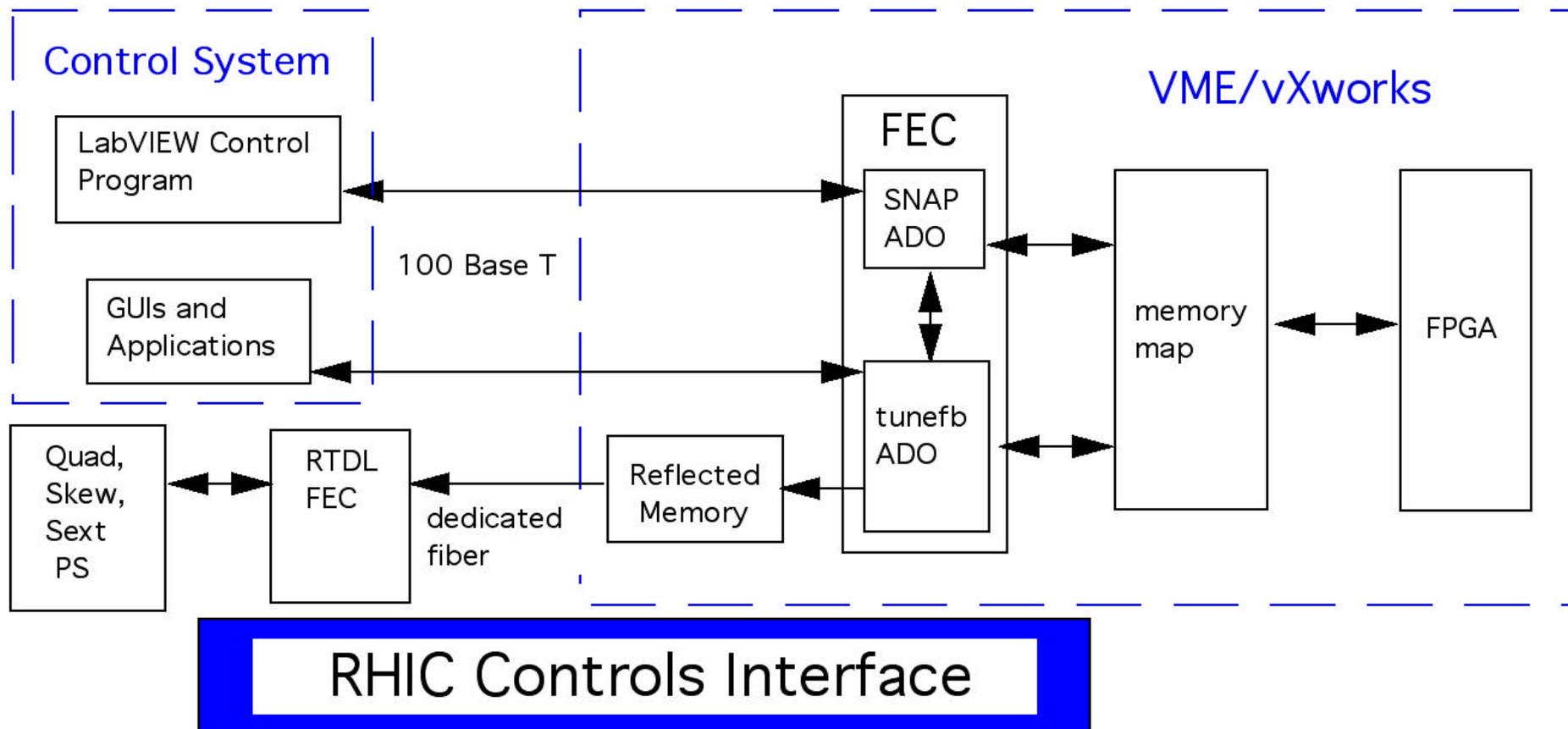


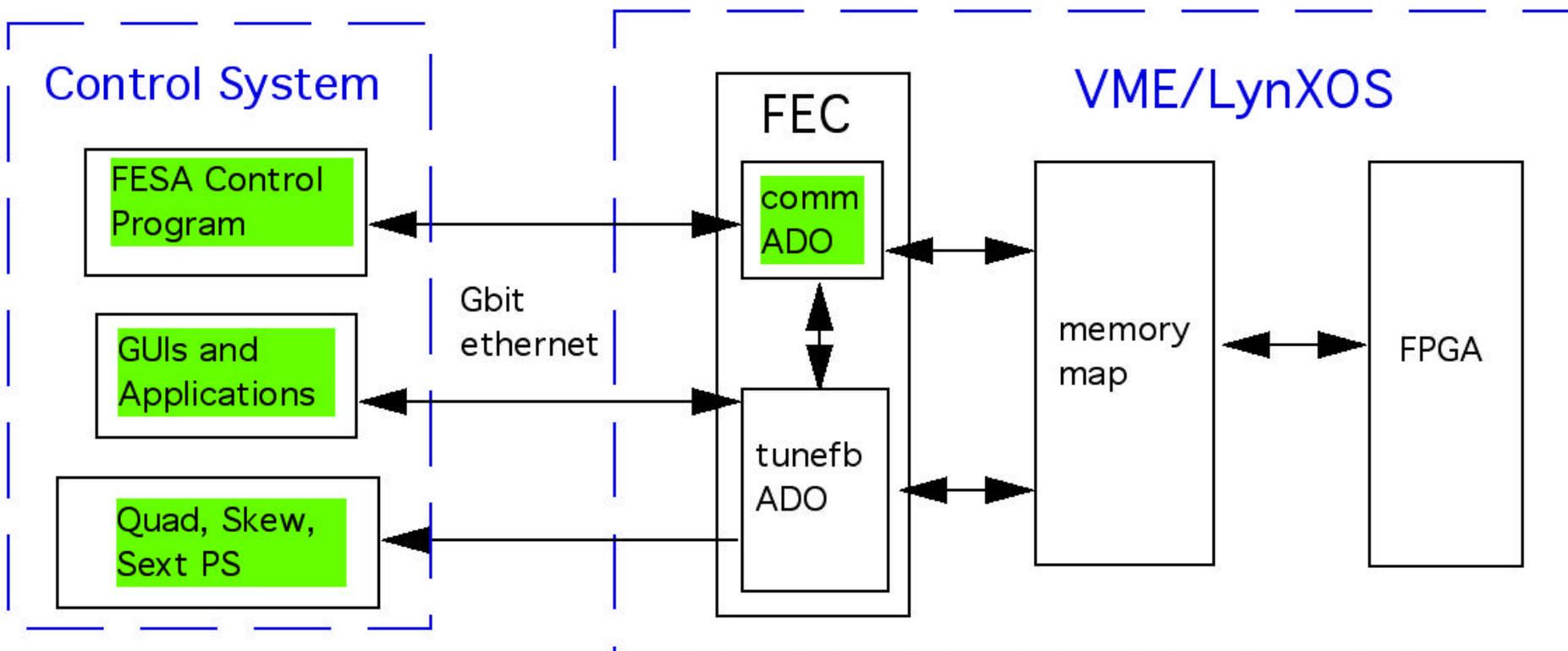


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LHC Controls Interface

LabVIEW/FESA Write Block



VME base offset	C variable	description
\$0000	cr	control register
\$0004	q_nom	nominal tune
\$0008	q_min	lower tune window limit
\$000C	q_max	upper tune window limit
\$0010	Ko	overall loop gain coefficient
\$0014	Kp	proportional gain
\$0018	Ki	integral gain
\$001C	Kd	derivative gain
\$0020	phase	phase offset [degrees]
\$0024	rps	ramp phase shift [deg/MHz]
\$0028	kicker_gain	kicker power amplifier gain [dB] (not in feedback loop)
\$002C	kick_limit	kicker maximum power limit [dBm]
\$0030	kick_loop_gain	kicker feedback loop gain
\$0034	I_requested	desired I value [digitizer counts]
\$0038	I_window	I window size [digitizer counts]
\$003C	pre_gain	signal path preamp gain [dB]
\$0040	pre_loop_gain	signal path preamp loop gain
\$0044	lock_multiple	ratio of Q/I for lock bit

Control Register Parameters



Control Register Parameters (plane base + \$0000) - written by LabVIEW/FESA

bit	parameter	description
0	restart search	1 = restart search, 0 = don't restart search
1	D to A write enable	1 = write D/A , 0 = don't write D/A
2	enable phase correction	1 = correct phase, 0 = don't correct phase
3	enable ramp phase correction	1 = ramp phase corr on, 0 = ramp phase corr off
4	60Hz filter on/off	1 = filter on, 0 = filter off
5	kicker amplifier on/off	1 = amplifier on, 0 = amplifier off
6	kicker amplifier on/off control	1 = from ADO, 0 = from LabVIEW
7	lock bit enable	1 = enable lock bit, 0 = disable lock bit
8	kicker drive loop enable	1 = enable drive loop, 0 = disable drive loop
9	preamp gain loop enable	1 = enable preamp gain loop, 0 = disable preamp gain loop

ADO Write Block

VME base offset	C variable	description
\$1000	sr	status register
\$1004	version	ADO software version
\$1008	I_corr	phase corrected I value
\$100C	Q_corr	phase corrected Q value
\$1010	counter	counter value
\$1014	DtoA	D to A value
\$1018	q	tune
\$101C	ampControlOut	power amplifier control
\$1020	tune_sigma	tune sigma
\$1024	new_lg	new loop gain
\$1028	new_kdl	new kicker drive level
\$102C		reserved
\$1030 - \$105C		virtual LCD
\$1060 - \$107C		data
\$1080 - \$1088		proportional, integral, derivative terms
\$108C	A	amplitude
\$1090	new_pre_gain	new preamp gain
\$1090 - \$1FFC		reserved
\$2000	acr	ADO control register
\$2004	rsf	relativistic slip factor
\$200C	B_rho	beam rigidity [T-m]
\$2010	beam_current	beam current [amp]

ADO Status and Control Registers



Status Register Parameters (plane base + \$1000) - written by ADO

bit	parameter	description
0	lock bit	0 = unlocked, 1 = locked
1	ring	0 = blue , 1 = yellow
2	axis	0 = horizontal, 1 = vertical
3	B_rho error	0 = B_rho OK, 1 = B_rho bad

ADO Control Register Parameters (plane base + \$2000) - written by ADO

0	amplifier power	1 = amplifier on, 0 = amplifier off
1	kicker drive loop enable	1 = enable drive loop, 0 = disable drive loop

FPGA Write Block



- not yet defined

Magnet Manager Application



- ADO provides
 - $q_1(q_x)$ and $q_2(q_y)$
 - $Q\xi_1$ and $Q\xi_2$
 - $r_1, r_1, \Delta\phi_1, \Delta\phi_1$
- Manager provides
 - feedforward capability on tune, chrom, coupling
 - feedback capability on tune, chrom, coupling

GUIs and Archiving



- GUIs are required for
 - $q_1(q_x)$ and $q_2(q_y)$
 - I_1, I_2, Q_1, Q_2
 - $Q\xi_1$ and $Q\xi_2$
 - $r_1, r_1, \Delta\phi_1, \Delta\phi_1$
- The capability of archiving data streaming to these GUIs is necessary

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Boundaries

- CERN
 - kicker amplifier, kicker, and pickup
 - Direct Diode Detection AFEs
 - Digitizer boards
 - DAB64 Boards
 - VME crate and crate computers for CERN installation
- LARP
 - VME crate and crate computers for LHC test installation at BNL
 - gate array programming
 - FEC programming
 - LabVIEW control program, collaboration on CERN equivalent
 - specification and testing of LHC TF Applications software
 - testing at RHIC, with and without beam
 - commissioning support

Summary



- Broad outline of overall architecture is in place
 - Details on PLL side are falling into place rapidly
 - Directly transferrable from BNL to CERN:
 - FPGA code
 - tune fb ADO
 - Porting to CERN required for:
 - LabVIEW to FESA
 - SNAP to comm ADO
 - Higher level support required for:
 - Magnet manager
 - GUIs and Archiving
- required to run PLL
- required for feedbacks and feedforwards