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## Functional Specification

# VME64x DIGITAL ACQUISITION BOARD FOR THE LHC TRAJECTORY AND CLOSED ORBIT SYSTEM

### Abstract

The LHC trajectory and closed orbit measurement system is based on a wide-band time normaliser (WBTN). This processes the analogue signals coming from the four-button pick-up to produce digitised position data at a rate of 40MHz. The Digital Acquisition Board (DAB), a VME64x standard board, whose functional specifications are described in this engineering specification, will be required to select, store, and pre-process this position data. The DAB is also foreseen to be used for other beam instrumentation acquisition systems such as the LHC Beam Loss Monitors, Fast Beam Current Transformers and Luminosity Monitors. The DAB will be designed at TRIUMF using these functional specifications, as part of the CERN/TRIUMF collaboration under the auspices of the Canadian contribution to the LHC.

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**History of Changes**

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0.1	2003-06-23	21	Creation of document	
	2003-11-07	all	Submission for approval	
	2003-11-18	10	Update of power consumption table to include fuse ratings for all power supplies.	
		11	Update of the JX1 and JX2 connector tables	
		12	Addition of $\pm 15V$ supplies to status register	
		14	Removal of row z on the P0 connector	
		14	Change of BLM outputs to open-collector outputs	
		2003-12-01	4	Update of nominal filling scheme
			6	Masked bunches should be disregarded by capture functions (not orbit functions)
			7	7 bytes (not 6) required for batch capture function
			10	Update of timing section to include BST and BOBR receiver and addition of a comment on UTC time-stamping
			15	Correction of MTM-JTAG correspondence
	15	Update of software section		
	18	Update of general layout		
	21	Update of front-panel layout		
1.0	2003-12-15	All	Final version	
			Released version	
2.0	2004-03-09	10	Control signals from the FPGA added to JX2-a5...8.	
		11	Table 2 modified to add the control signals.	
		13	Command register includes Control [0...3].	

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## 1. INTRODUCTION

The LHC trajectory and closed orbit measurement system is based on a wide band time normaliser (WBTN) for the acquisition of 40MHz digitised position data from an analogue pick-up signal. The Digital Acquisition Board (DAB) shall be responsible for the selection, sorting, pre-processing and validation of this data. It is also foreseen to use this board as part of the fast beam current transformer (FBCT) acquisition system. It shall be capable of functioning in three parallel modes:

- 'Orbit' - providing a continuous, real-time closed orbit measurement.
- 'Capture' - providing turn-by-turn measurement for selected/all bunches/batches.
- 'Post-Mortem' - providing a history of the beam orbit and turn-by-turn position.

In addition, asynchronous operation shall be foreseen, where all the above modes function without the need for synchronised external timing. Each DAB shall perform the above functions for both the horizontal and vertical plane. All DAB functionalities shall be envisaged for 12bit data. Since the SPS will be used for testing the DAB module, it should also be capable of functioning using SPS parameters. In total about 1000 DABs will be needed for the LHC rings and about 120 for the transfer lines.

## 2. GENERAL SPS AND LHC PARAMETERS

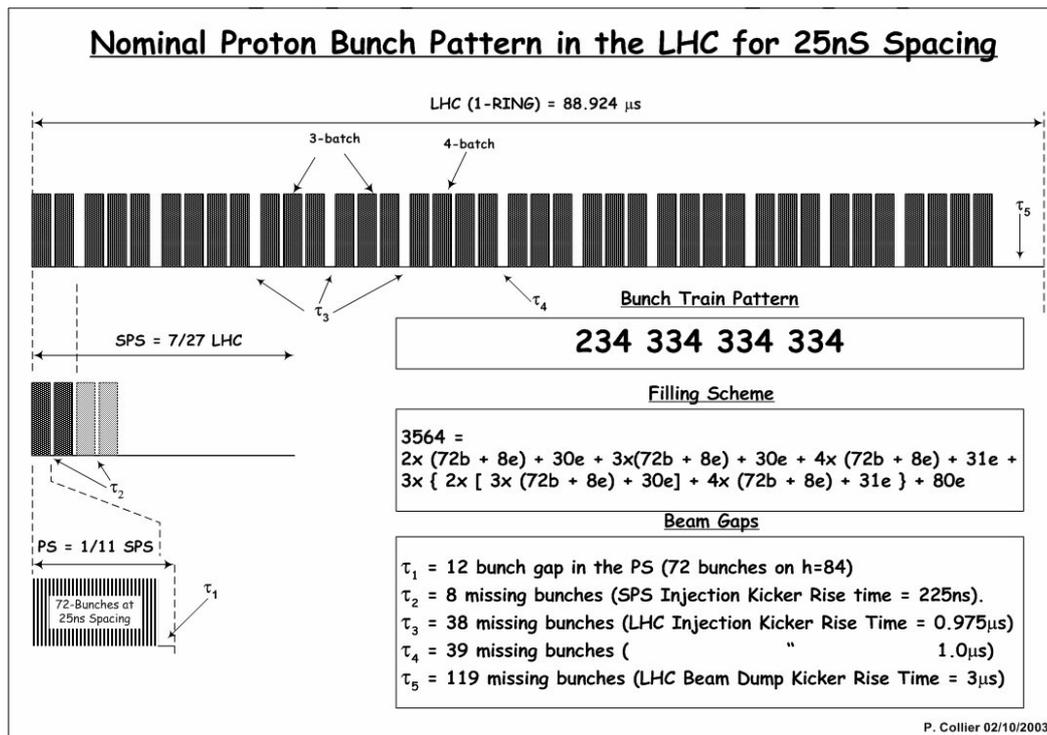


Figure 1: The nominal LHC filling scheme for proton operation

The nominal SPS and LHC bunch spacing is 24.95ns, which for the SPS represents a revolution period of 23.055 $\mu$ s divided by a possible 924 slots, or for the LHC a period of 88.924 $\mu$ s divided by a possible 3564 slots.

For proton-proton collisions, a total of 2808 bunches are injected in 12 batches into each ring. Each of these batches will consist of either 2, 3 or 4 PS batches containing

72 bunches. The injection sequence presently foreseen is 234-334-334-334, as shown in figure 1. Since this injection scheme is liable to change before, during and after the commissioning of the LHC, it shall be possible to define and modify the batch structure and batch sequence via the DAB software.

### 3. SYSTEM LAYOUT

The LHC trajectory and closed orbit system can be split into four main components:

- Beam Position Monitor (BPM). The majority of the BPMs are located in the arc regions of the LHC, inside the cryostat of the Short Straight Section (SSS) containing the quadrupoles. These monitors are based on button electrodes and will typically operate at temperatures between 5K and 25K. The signal from each button electrode will be transmitted to a warm feedthrough on the cryostat using cryogenic, semi-rigid coaxial cables. Each quadrupole will be equipped with two BPMs, one for each of the LHC rings. The SPS to LHC transfer lines will each contain 26 horizontal and 27 vertical pick-ups, with the signals processed by the same electronics as used in the LHC.
- Wide Band Time Normaliser (Front-end). The front-end of the WBTN will convert the signals from one plane of a BPM (2 electrodes) into a corresponding position measurement for that plane. These front-ends are envisaged to be placed beneath the SSS cryostats containing the BPMs. The radiation dose in these regions is estimated at around 12Gy per year. There will be four WBTN front-end modules per SSS (one for each plane for both rings). The acquisition is auto-triggered, eliminating the need for external timing in the tunnel. Using wide band time normalisation, the position data can be represented as the time difference between the rising edges of two pulses. Fibre optic transmission will therefore be used to send these pulses from the front-end unit to the digitisation module, located outside the tunnel in a radiation free environment.
- Wide Band Time Normaliser (Digitisation). This integrates the time difference between the two rising edges of the fibre-optically transmitted pulses, before digitisation using a 10bit (or 12bit), 40MHz ADC. The digitisation module of the WBTN will take the form of a mezzanine card, with two of these per DAB module (one for each plane). This will allow a single DAB card to treat the data from one BPM (horizontal and vertical). As outputs, the WBTN will provide the DAB with 10bits (or 12bits) of data, a data-valid-strobe bit, and a data-in-range bit. As inputs, the WBTN will require the DAB to provide the necessary powering.
- Digital acquisition Board (DAB). This will process the 40MHz data from the WBTN, and is the subject of this specification. A proposed topology for the various DAB functions is provided in Appendix A.

### 4. ORBIT ACQUISITION

The orbit measurement system will be used to calculate the orbit correction in the LHC. On reception of a 'start orbit capture' trigger (external or via software), the DAB shall therefore produce the accumulated position measurement:

- of all bunches over up to 870 turns - 'Global Orbit Acquisition'.
- for up to 13 individual batches over up to 870 turns. The additional batch is foreseen for FBCT measurements during the "no-beam" time ( $\tau_5$  in figure 1).
- for 16 user selectable bunches over up to 870 turns.

The 870 turns correspond to  $\sim 20$ ms for the SPS which, based on LEP experience, has proven to be very efficient in rejecting any 50Hz mains ripple. The number of turns per orbit acquisition shall therefore be settable via software (1-1024).

It shall be possible to apply a bunch mask to any of the 3564 bunch slots. A masked slot shall be disregarded for all capture functions specified in section 5. It shall be possible to define and change the batch structure used when performing an orbit acquisition. Only valid WBTV data shall be accumulated, with a separate count carried out of any acquisition errors.

In addition, each 'Global Orbit Acquisition' shall be accompanied by a measure of the spread of the collected data (standard deviation), to be used as a check on the validity of the acquired data (see section 4.2).

On completion of an acquisition a VME interrupt shall be created.

#### 4.1 MEMORY ORGANISATION

- 1.** A global orbit acquisition consists of 22 bytes of data:
  - 5 bytes for the sum of the horizontal position ADC Data in up to 1024 turns.
  - 3 bytes for the number of valid horizontal acquisitions in up to 1024 turns.
  - 3 bytes for the number of horizontal acquisition errors in up to 1024 turns.
  - 5 bytes for the sum of the vertical position ADC Data up to 1024 turns.
  - 3 bytes for the number of valid vertical acquisitions in up to 1024 turns.
  - 3 bytes for the number of vertical acquisition errors in up to 1024 turns.
  
- 2.** Each of the 13 batch orbit acquisitions consists of 24 bytes of data:
  - 5 bytes for the sum of the horizontal position ADC Data in up to 1024 turns.
  - 3 bytes for the number of valid horizontal acquisitions in up to 1024 turns.
  - 3 bytes for the number of horizontal acquisition errors in up to 1024 turns.
  - 5 bytes for the sum of the vertical position ADC Data in up to 1024 turns.
  - 3 bytes for the number of valid vertical acquisitions in up to 1024 turns.
  - 3 bytes for the number of vertical acquisition errors in up to 1024 turns.
  - 2 bytes for batch identification and status bits.
  
- 3.** Each of the 16 single bunch orbit acquisitions consists of 12 bytes of data:
  - 3 bytes for the sum of the horizontal position ADC Data in up to 1024 turns.
  - 2 bytes for the number of valid horizontal acquisitions in up to 1024 turns.
  - 3 bytes for the sum of the vertical position ADC Data in up to 1024 turns.
  - 2 bytes for the number of valid vertical acquisitions in up to 1024 turns.
  - 2 bytes for the bunch identification number and status bits.

#### 4.2 GLOBAL ORBIT HISTOGRAMMING

In order to obtain the distribution of the data within one global orbit acquisition, a method based on the histogramming of the data is proposed. A 12bit address is used to locate the 'memory bin' of the histogram that corresponds to the incoming, 40MHz data. The value at this location is then incremented by one (see figure 1). After a complete global orbit acquisition this memory histogram will then contain the distribution of all the acquired data, and can be used for data validation.

A global orbit histogram acquisition will consist of the following:

- 4096 memory locations of 22bits for the Horizontal histogram over 1024 turns.
- 4096 memory locations of 22bits for the Vertical histogram over 1024 turns.

Since a normal acquisition will be limited to a small part of the reserved histogram memory, the address corresponding to the minimum and maximum non-empty 'memory bin' shall also be stored. This will considerably reduce the amount of data that has to be read over the VME bus.

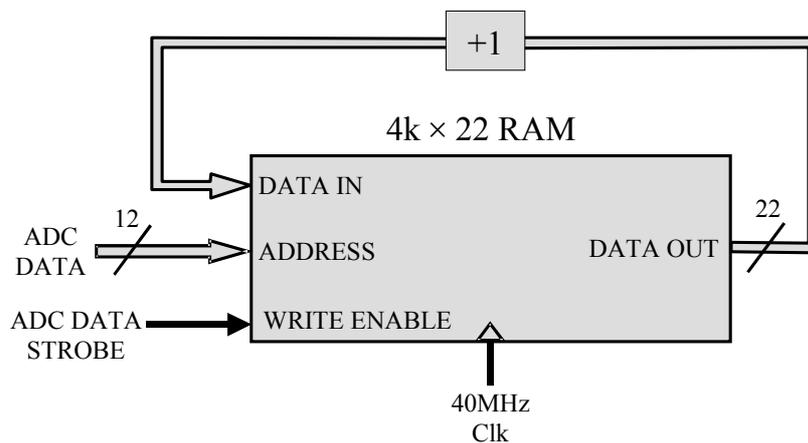


Figure 1. Implementation example of Global Orbit histogramming.

### 4.3 LOOK-UP TABLE FOR ONLINE DATA CORRECTION

A 12-bit look-up table shall be implemented for the raw data coming from the mezzanine card, irrespective of whether the data is destined for global orbit or capture (see section 5) acquisition. For the WBTN mezzanine this will take into account the 3<sup>rd</sup> order correction polynomial of the wide band time normaliser, which is determined by calibration. It shall be possible to bypass the use of this table for cases where the acquisition of the raw data is important (e.g. WBTN calibration). For the fast beam current transformer it is important that the switching from using the look-up table to bypassing the table can occur in 25ns, since only every other input data will require correction. For the fast beam current transformer the choice of look-up table or bypass will be indicated using the active integrator status bit.

### 4.4 ONLINE OFFSET SUBTRACTION (FBCT)

For the fast beam current transformer (FBCT) to be able to use the same routines as the beam position system, online offset subtraction has to be performed on all incoming data. The FBCT acquisition mezzanine will have data coming from 2 integrators, each of which has a constant offset. The currently active integrator will be indicated using an additional status bit to the ADC strobe and in-range bits. The DAB shall be capable of subtracting the corresponding offset.

## 5. TURN-BY-TURN POSITION ACQUISITION

In parallel to the real-time data processing of the orbit, it shall be possible to use the DAB to obtain turn-by-turn position information for specific bunches or batches in a random acquisition mode, henceforth referred to as 'capture' mode. The user shall have the possibility to select from the following modes of acquisition:

1. Select N slots among the 3564, for T turns, where  $N \times T \leq 100000$ .  
This can be used to dump all slots for a short period of time or to trace a few selected bunches over a longer time period, where  $N \leq 3564$  and  $T \leq 100000$ .  
e.g. 100 bunches for at least 1000 turns or 1 bunch for 100000 turns.
2. The sum, valid acquisitions count and error count in a given batch for B selected batches, for T turns, where  $B \times T \geq 13000$ .  
e.g. the sum of 13 individual batches for at least 1000 turns.
3. The sum, valid acquisitions count and error count of all bunches for T turns, where  $T \geq 1000$

In addition it shall be possible to set a capture acquisition turn divider which will allow the above mentioned acquisitions to be performed every 1-128 turns, with the total number of acquisitions remaining unchanged. On completion of an acquisition an interrupt shall be sent to the VME host.

## 5.1 MEMORY ORGANISATION

1. For a single bunch, one measurement consists of 8 bytes of data:
  - 4 bytes for horizontal position data, consisting of:
    - the bunch number (1-3564)  $\Rightarrow$  12bits.
    - the 12bit ADC Data.
    - strobe present, in-range bit, extra status bit (BCT)  $\Rightarrow$  3bits.
  - 4 bytes for vertical position data, consisting of:
    - the bunch number (1-3564)  $\Rightarrow$  12bits.
    - the 12bit ADC Data.
    - strobe present and in-range bits, extra status bit (BCT)  $\Rightarrow$  3bits.
2. For a single batch, one measurement consists of 14 bytes of data:
  - 7 bytes for the horizontal position data, consisting of:
    - the batch number (1-13)  $\Rightarrow$  4bits.
    - the sum of the 12bit ADC data for all bunches in a batch  $3564 \times 4096 = 24$ bits.
    - the horizontal bunch count (valid data only)  $3564 = 12$ bits.
    - the horizontal error count  $3564 = 12$ bits.
  - 7 bytes for the vertical position data, consisting of:
    - the batch number (1-13)  $\Rightarrow$  4bits.
    - the sum of the 12bit ADC data for all bunches in a batch  $3564 \times 4096 = 24$ bits.
    - the vertical bunch count (valid data only)  $3564 = 12$ bits.
    - the vertical error count  $3564 = 12$ bits.
3. For the average of all bunches one measurement consists of 12 bytes of data:
  - 6 bytes for the horizontal position data consisting of:
    - the sum of the 12bit ADC data for all bunches  $3564 \times 4096 = 24$ bits.
    - the horizontal bunch count (valid data only) (1-3564)  $\Rightarrow$  12bits.
    - the horizontal error count (1-3564)  $\Rightarrow$  12bits.
  - 6 bytes for the vertical position data consisting of:
    - the sum of the 12bit ADC data for all bunches  $3564 \times 4096 = 24$ bits.
    - the vertical bunch count (valid data only) (1-3564)  $\Rightarrow$  12bits.
    - the vertical error count (1-3564)  $\Rightarrow$  12bits.

## 6. POST-MORTEM

In order to diagnose and understand beam loss or sudden beam dumps in the LHC all beam instrumentation will have to provide so-called 'post-mortem' information. This records the last movements of the beam prior to total beam loss or a beam dump. The requirements are for:

- the last 1000 turns of average position data (i.e. the average of all bunches every turn). In order to store this, the DAB shall retain the sum of all bunches (3 bytes), and the number of valid bunches (12bits) and error count (12bits) acquired for each of the 1000 turns (see section 5.1 mode 3). This implies a total memory of 2×6kBytes for horizontal and vertical acquisitions.
- The last 1000 global orbit acquisitions. Each orbit acquisition contains the sum of all bunches for up to 1024 turns (5 bytes), the total number of bunches registered (3 bytes) and the total error count (3 bytes). This implies a total memory of 2×11kBytes for horizontal and vertical acquisitions.

This function shall be duplicated for two different start and freeze triggers:

- Post Mortem start and freeze
- Auxiliary post-mortem start and freeze

The start and freezing of the acquisition shall be possible via hardware signals from the P0 connector (see section 11.5), or via software. Book-keeping shall be implemented to keep tabs on the start and end of the circular buffers.

## 7. ASYNCHRONOUS MODE

In order to avoid the need for beam synchronous timing in the LHC tunnel, the calibration of the system will be carried out using a local oscillator on the WBTN front-end. The DAB shall therefore be capable of operating in an asynchronous mode, where it is not reliant on the normal 40MHz bunch clock and 11kHz revolution frequency (43kHz for the SPS). Instead it shall use the 'data-valid strobe' provided by the WBTN as its reference clock. This mode will also be used during the setting-up period with beam, where there is likely to be no synchronism between the beam and the external timing. Four possible asynchronous timing scenarios are foreseen:

- a continuous 40MHz (25ns), 13.33MHz (75ns) or 8MHz (125ns) clock.
- a single clock every 89µs (23µs for the SPS).
- a burst of 72 clocks every 89µs (23µs for the SPS).
- a single burst of between 1 and 288 clocks.

For all cases where there is a continuous clock, the DAB shall be capable of functioning as if the signals were derived from the beam, i.e. the Orbit, Capture and Post Mortem modes shall all work as foreseen. In the special case of a single burst of clocks only the Capture mode is required to function.

## 8. DAB - WBTN INTERFACE

Each DAB module shall be a host to two WBTN digitisation mezzanine cards (see Annex B, figure B1). The dimensions and position of these mezzanine cards are shown in Annex B1, figure B2. All of these dimensions relate to a standard *VME Rev C. IEEE 1014-1997 size B* DAB card (see section 9). Figure B2 also identifies the regions where the DAB component height is limited to 1.7mm or 3.5mm, in all other locations the maximum component height shall be 6.5mm.

Each mezzanine card shall be connected via two HARWIN M50-4322005 20-pin connectors, the layouts of which are shown in Annex B, figure B3. The connectors for each card shall be known as JX1 (vertical connector) and JX2 (horizontal connector), where X denotes the card ( $X=1 \rightarrow$  lower,  $X=2 \rightarrow$  upper). The pin-out for these connectors is the same for each card and is specified in table 2.

- Connector JX1 will be used to supply all the relevant power to the mezzanine card. The estimated power consumption of a single mezzanine card is summarised in table 1. Separate fuses shall be installed on the DAB card for each of these power supplies and for each mezzanine card.
- Pins a15,a16,b15,b16 are for testing the WBTN mezzanine cards and have no connections with the DAB.
- Pins a/b9→a/b20 on the JX2 connector will supply the DAB with 12-bit inputs.
- Pin b8 on the JX2 connector will supply the DAB with an in-range bit.
- Pin b7 on the JX2 connector will supply the DAB with an ADC strobe (data valid on the falling edge).
- Pins b6 on the JX2 connector is defined as an input to the mezzanine, and shall provide a TTL level external trigger on the next turn clock from the FPGA on request.
- Pins a5→a8 on the JX2 are TTL control inputs to the mezzanine, and must be connected to the FPGA with  $1k\Omega$  series resistors.
- Pin b5 on the JX2 connector will supply the DAB with the integrator selection bit (used for the fast BCT application to subtract offsets).
- Pins a/b1 provide the mezzanine with the buffered Turn clock LVDS signal from the P0 connector (pins a12/13).
- Pins a/b2 provide the mezzanine with the buffered 40MHz clock LVDS signal from the P0 connector (pins a16/17).
- Pins a/b3 provide the mezzanine with the delayed Turn clock signal from the FPGA. This shall also be implemented as LVDS, with the relevant (horizontal or vertical) delayed Turn clock being routed to the appropriate J12 or J22 connector.
- Pins a/b4 provide the mezzanine with the delayed 40MHz clock signal from the FPGA. This shall also be implemented as LVDS, with the relevant (horizontal or vertical) delayed 40MHz clock being routed to the appropriate J12 or J22 connector.

Buffers for all the digital inputs and outputs will have to be implemented on the DAB, since none are foreseen on the WBTN mezzanine.

	DAB64x VME supplies		WBTN Power Requirement (1 Mezzanine card)					Additional Supplies (1 Mezzanine card)	
	Digital		Analogue			Digital		Analogue	
	+3.3V	+5V	-5.2V	-2V	+5V	+3.3V	+5V	+15V	-15V
<b>Consumption</b>	NA	NA	≈ 810mA	≈ 570mA	≈ 310mA	≈ 100mA	≈ 80mA	≈ 100mA	≈ 100mA
<b>Fuse Value</b>	2600mA	1100mA	1100mA	1100mA	500mA	500mA	500mA	500mA	500mA
<b>Total Power Dissipation ≈ 7.6W</b>									

Table 1: Fuse requirements for main board protection and for each mezzanine card.

## DATA ACQUISITION BOARD JX1 JX2 pin allocation

JX1			JX2		
	a	b		a	b
1	+15V	+15V	1	Turn Clk +	Turn Clk -
2	+15VRET	+15VRET	2	40MHz +	40MHz -
3	-15VRET	-15VRET	3	Delayed Trn Clk +	Delayed Trn Clk -
4	-15V	-15V	4	Delayed 40MHz +	Delayed 40MHz -
5	-5.2VRET	-5.2VRET	5	Control 0	FBCT Integrator #
6	-5.2VRET	-5.2VRET	6	Control 1	Ext Trig
7	-5.2V	-5.2V	7	Control 2	Strobe
8	-5.2V	-5.2V	8	Control 3	IR
9	-2VRET	-2VRET	9	DGnd	D11
10	-2VRET	-2VRET	10	DGnd	D10
11	-2V	-2V	11	DGnd	D9
12	-2V	-2V	12	DGnd	D8
13	+5V	+5V	13	DGnd	D7
14	+5VRET	+5VRET	14	DGnd	D6
15	Unconnected	Unconnected	15	DGnd	D5
16	Unconnected	Unconnected	16	DGnd	D4
17	DGnd	DGnd	17	DGnd	D3
18	+5VD	+5VD	18	DGnd	D2
19	DGnd	DGnd	19	DGnd	D1
20	+3.3VD	+3.3VD	20	DGnd	D0

Table 2: The pin allocation of the JX1 and JX2 connectors for the WBTN mezzanine cards.

## 9. DAB - VME INTERFACE

The DAB module shall:

- conform to VME64x specifications as described in ANSI/VITA 1-1994 and ANSI/VITA 1.1-1997 [see 1,2,3]. The VME64x standard includes 160-pin P1 and P2 connectors, a 114-pin P0 connector, geographical addressing, voltage pins for 3.3V, a test and maintenance bus, and an EMC front panel.
- use D32 A32 or D64 A64 transfer mode.
- be fully VME slave compatible
- be mapped into the VME A32 standard space (AM = 09,0B, 0D or 0F)
- allow the base address offset to be set using 5-bit on-board switches or via the VME64x Geographical Addressing protocol [see 3]. The memory space for VME A32 accesses start at address 0x00000000. Each DAB module can use up to 128Mbytes of memory, and a maximum of 20 DAB modules must be independently selectable. The address decoding shall therefore be done on address bits: A32→A28. This means that DAB modules in the address space 0x00000000 to 0x1F000000 can be selected.
- be capable of addressing without wait-state
- have a D64 block transfer capability (BLT slave) to ensure fast data reading.
- have a single programmable level interrupter, with daisy-chain management.
- allow the interrupt source to be selected from any local status. For example at the end of an acquisition sequence.

- have all programmable parts (FPGA, EPLD) accessible via both the VME and a JTAG interface for command writing and status reading.

## 10. TIMING AND SYNCHRONISATION

All internal synchronisation signals depend on the revolution frequency, also known as 'Frev' or 'Turn Clock', of 11.2455kHz for LHC (43.375kHz for SPS), and the 40MHz bunch synchronous timing. These signals will be provided via the Beam Synchronous Timing (BST), based on the Timing, Trigger and Control system protocol [4]. A receiver module (BOBR) in each VME64x chassis will retrieve the 40MHz bunch clock, the turn clock and will decode any message information and re-transmit them via the P0 connector (on row d & e - see section 11.5) as hardware triggers, or make them available to the host CPU. In addition to the external timing the DAB64x shall be capable of generating its own independent 40MHz and turn clock signals (referred to as internal timing).

The DAB64x shall be capable of functioning in any of the following timing modes:

- Turn Clock and 40MHz external (provided by the BST system). - DEFAULT
- 40MHz external and Turn Clock internal via clock counter.
- Turn Clock external and 40MHz internal.
- Turn Clock and 40MHz internal.

### 10.1 TURN CLOCK AND 40MHZ PHASE ADJUSTMENT

The digitisation module of the WBTN will provide a 'data-valid strobe' that shall be used to clock in the data. The horizontal and vertical WBTN mezzanine cards will provide separate strobes, which in the case of the transfer lines can arrive several tens of nanoseconds apart. It is therefore suggested that the DAB treat horizontal and vertical data separately, storing them in different memories.

The DAB module shall provide a means of setting a separate turn clock delay and 40MHz phase adjustment for the horizontal and vertical data. The turn clock delay shall be capable of being adjusted by up to 3564 40MHz clock pulses.

The 40MHz phase shall be capable of being adjusted in steps of  $\sim 2$ ns (bunch clock phase adjust) to provide a good phase adjustment with the WBTN strobe.

### 10.2 UTC TIME-STAMPING

No UTC time-stamping of the acquisition or post mortem memories needs to be foreseen for each individual DAB. The correspondence between acquisition times and UTC will be provided by the BST system and the necessary time-stamping will be handled by the host CPU.

## 11. DAB SPECIFIC FEATURES

### 11.1 STATUS REGISTER (READ ONLY)

The status register shall provide the following information:

- Orbit acquisition running/stopped.
- Capture acquisition running/stopped.

- Post Mortem running/stopped.
- External Turn Clock detected/not detected.
- External 40MHz detected/not detected.
- Machine selection status LHC/SPS (set via jumper)
- CPLD device configuration status OK/not configured.
- WBTN power supply status (+15V, +5V, +5VD, +3.3VD, -2V, -5.2V, -15V).

## 11.2 COMMAND REGISTER (READ/WRITE)

The command register shall provide the following functionalities:

- Set timing mode, either:
  - Turn Clock and 40MHz external.
  - 40MHz external and Turn Clock internal.
  - Turn Clock external and 40MHz internal.
  - Turn Clock and 40MHz internal.
- Start orbit acquisition.
- Start capture acquisition.
- Start post mortem acquisition.
- Freeze post mortem acquisition.
- Control [0...3].
- Single external trigger (see JX2 connector, section 8).

## 11.3 FRONT-PANEL

- EMC protection
  - The front panel shall comply with VME64x specifications regarding EMC protection.
- Fibre optic Inputs (Holes only)
  - 2 × E2000 connectors for the WBTN signals
- MMCX Inputs (Holes only)
  - 2 × Electrical input for the WBTN digitisation mezzanines
- MMCX 50Ω Outputs (Holes only)
  - 2 × WBTN optical input monitoring.
  - 2 × WBTN analogue position output.
- LEMO Inputs (TTL Level / 50Ω)
  - Turn Clock           – capture start
  - 40MHz                – orbit start
- LEMO Outputs (TTL Level / 50Ω)
  - 2 x Multiplexed outputs from the FPGA:
 

<ul style="list-style-type: none"> <li>• ADC strobe (HOR &amp; VER)</li> <li>• Phase corrected 40MHz (HOR &amp; VER)</li> <li>• Delayed turn clock (HOR &amp; VER)</li> <li>• P0 40MHz</li> <li>• P0 turn clock</li> </ul>	<ul style="list-style-type: none"> <li>• P0 capture start</li> <li>• P0 post-mortem start</li> <li>• P0 post-mortem freeze</li> <li>• Capture running</li> <li>• Orbit running</li> </ul>
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- P0 orbit start
- LED Indicators
  - VME access
  - Device configured
  - Orbit Acquisition running
  - Capture Acquisition running
  - Power supply statuses
  - Post Mortem running
  - Asynchronous mode on
  - Selected 40MHz input present
  - Selected Turn Clock input present

#### 11.4 ON BOARD CONNECTORS AND FUSES

- 4 x HARWIN M50-4322005 20-pin connector (see section 8 and Appendix A).
- SPS/LHC machine selection switch.
- 10 pin JTAG interface connector (TAP) conforming to ALTERA ByteBlaster specifications.
- 38 pin Mictor connector for connecting a HP analyser. This may be used to validate the card by configuring the FPGA to route relevant signals to this connector.
- Protection fuses for the VME 5V and 3.3V supplies must be installed (see Table 1, section 8).

#### 11.5 P0 CONNECTOR

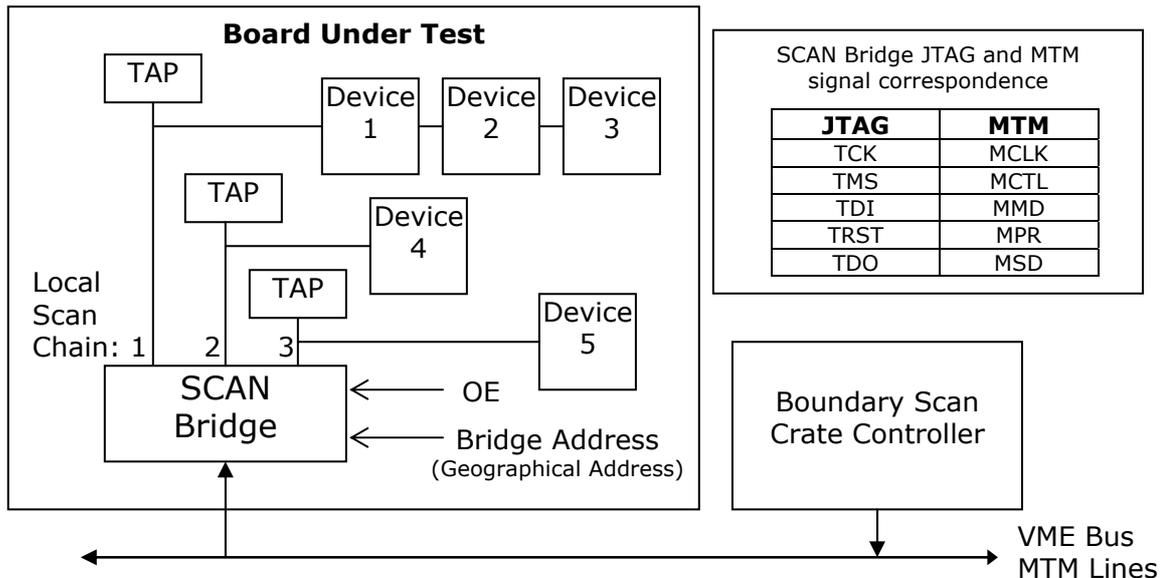
Pin	Row a	Row b	Row c	Row d	Row e	Row f
1	BLMin1	-5V2RET	-5V2RET	Capture Start	Post Mortem Start	GND
2	BLMin2	-5V2RET	-5V2RET	Auxiliary d2	Post Mortem Freeze	GND
3	BLMin3	-5V2RET	-5V2RET	Auxiliary d3	Auxiliary PM Start	GND
4	BLMin4	-5V2	-5V2	Auxiliary d4	Auxiliary PM Freeze	GND
5	BLMout1	-5V2	-5V2	Auxiliary d5	Orbit Start	GND
6	BLMout2	-5V2	-5V2	Auxiliary d6	Auxiliary e6	GND
7	BLMout3	-2VRET	-2VRET	Auxiliary d7	Auxiliary e7	GND
8	BLMout4	-2VRET	-2VRET	Auxiliary d8	Auxiliary e8	GND
9	Unused	-2V	-2V	Unused	Unused	GND
10	Unused	-2V	-2V	Unused	Unused	GND
11	Unused	Unused	Unused	Unused	Unused	GND
12	Unused	+5V	+5V	BS0	LVDS Turn clock Delay +	GND
13	Unused	+5V	+5V	BS1	LVDS Turn clock Delay -	GND
14	Unused	+5VRET	+5VRET	BS2	Unused	GND
15	Unused	+5VRET	+5VRET	BS3	Unused	GND
16	Unused	+15V	+15V	BS4	LVDS 40 MHz Clock +	GND
17	Unused	+15VRET	+15VRET	BS5	LVDS 40 MHz Clock -	GND
18	Unused	-15VRET	-15VRET	BS6	Unused	GND
19	Unused	-15V	-15V	BS7	Unused	GND

Table 3: The pin allocation for the DAB-P0 connector.

The following inputs and outputs have a buffered hardware connection to the main processing FPGA. All inputs (a1-a4, d1-d8, d12-d19, e1-e8) are TTL level inputs. The BLM outputs (a5-a8) shall be open-collector outputs.

## 11.6 JTAG INTERFACE

The DAB shall use a SCAN bridge, Type National Semiconductor SCANPSTA111 or similar, to interface the Multi-drop Test and Maintenance Bus (MTM-Bus IEEE 1149.5 Standard) to a maximum of 3 on-board JTAG chains. The SCAN Bridge outputs can be



tri-stated via the OE input strap to allow an alternate test master to take control of the local TAPs (e.g. direct programming or testing from a PC). A schematic implementation of such boundary scan architecture is shown in fig 2. For more information see [5].

Figure 2. Schematic of SCAN Bridge JTAG interface.

## 12. SOFTWARE

TRIUMF shall deliver the necessary software for the verification of the low-level functionalities of the DAB64x card. This software is not intended to be the APIs to higher level applications.

TRIUMF shall provide a standard LYNXOS device driver that allows all available registers on the DAB64x board to be accessed. This driver shall be developed using the "device driver generator" developed at CERN. A corresponding C-library shall be developed for higher level control. For initial card testing and debugging a simple Perl script GUI application shall be provided along with a C-language server using the CERN SL-Equip communication protocol.

CERN will be responsible for producing all the software intended for the final operation of the card and its linking with higher level applications.

## 13. REFERENCES

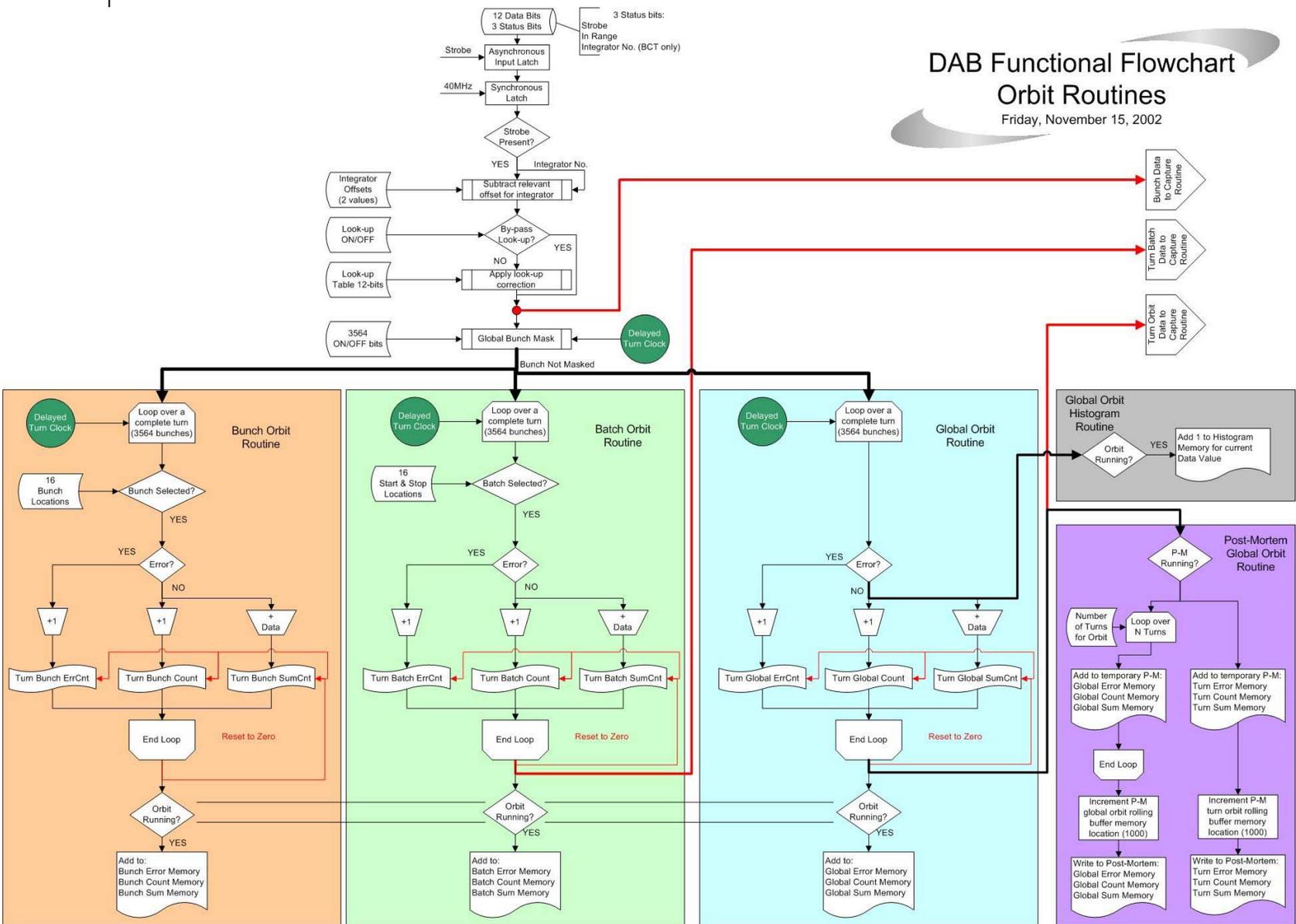
- [1] <http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/VMEbus/index.html>
- [2] <http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/VMEbus/standards/Av1.pdf>

- [3] <http://atlas.web.cern.ch/Atlas/GROUPS/FRONTEND/VMEbus/standards/Av1dot1.pdf>
- [4] <http://ttc.web.cern.ch/TTC/intro.html>
- [5] <http://www.national.com/appinfo/scan/>

## APPENDIX A – ACQUISITION FLOWCHARTS

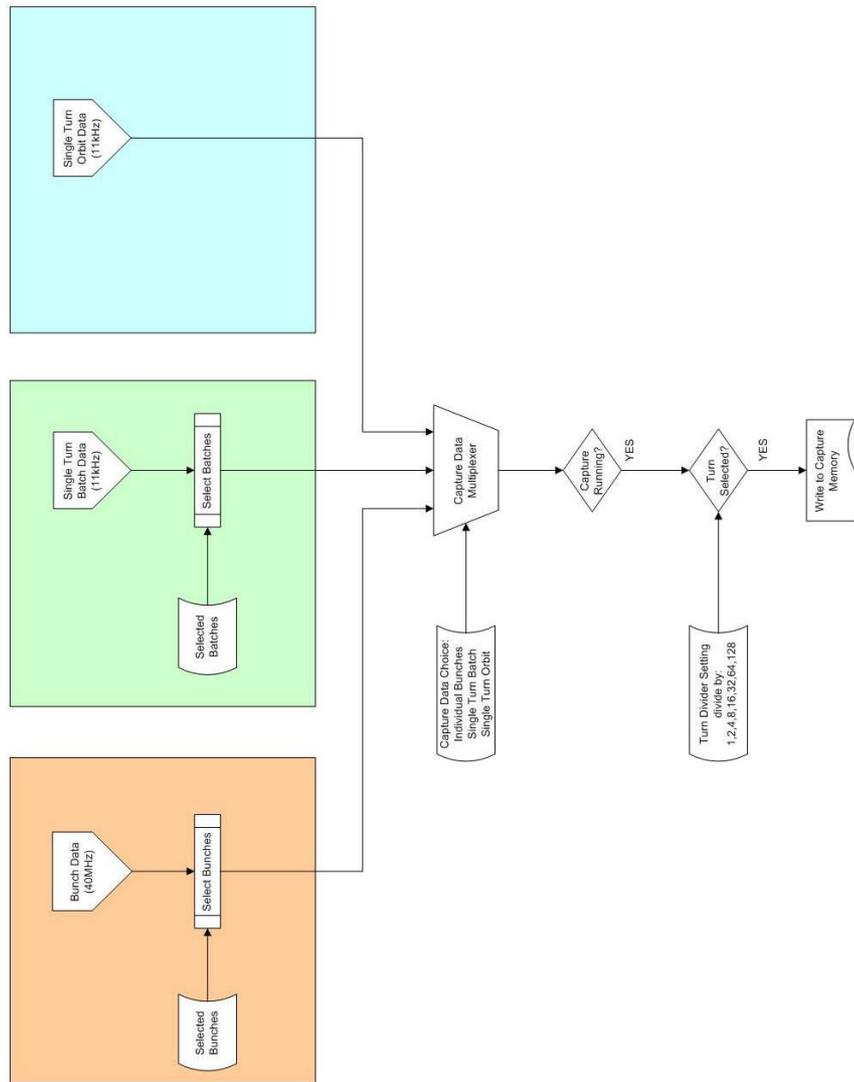
### DAB Functional Flowchart Orbit Routines

Friday, November 15, 2002



# DAB Functional Flowchart Capture Routines

Friday, November 15, 2002



## APPENDIX B – CONSTRUCTION DETAILS

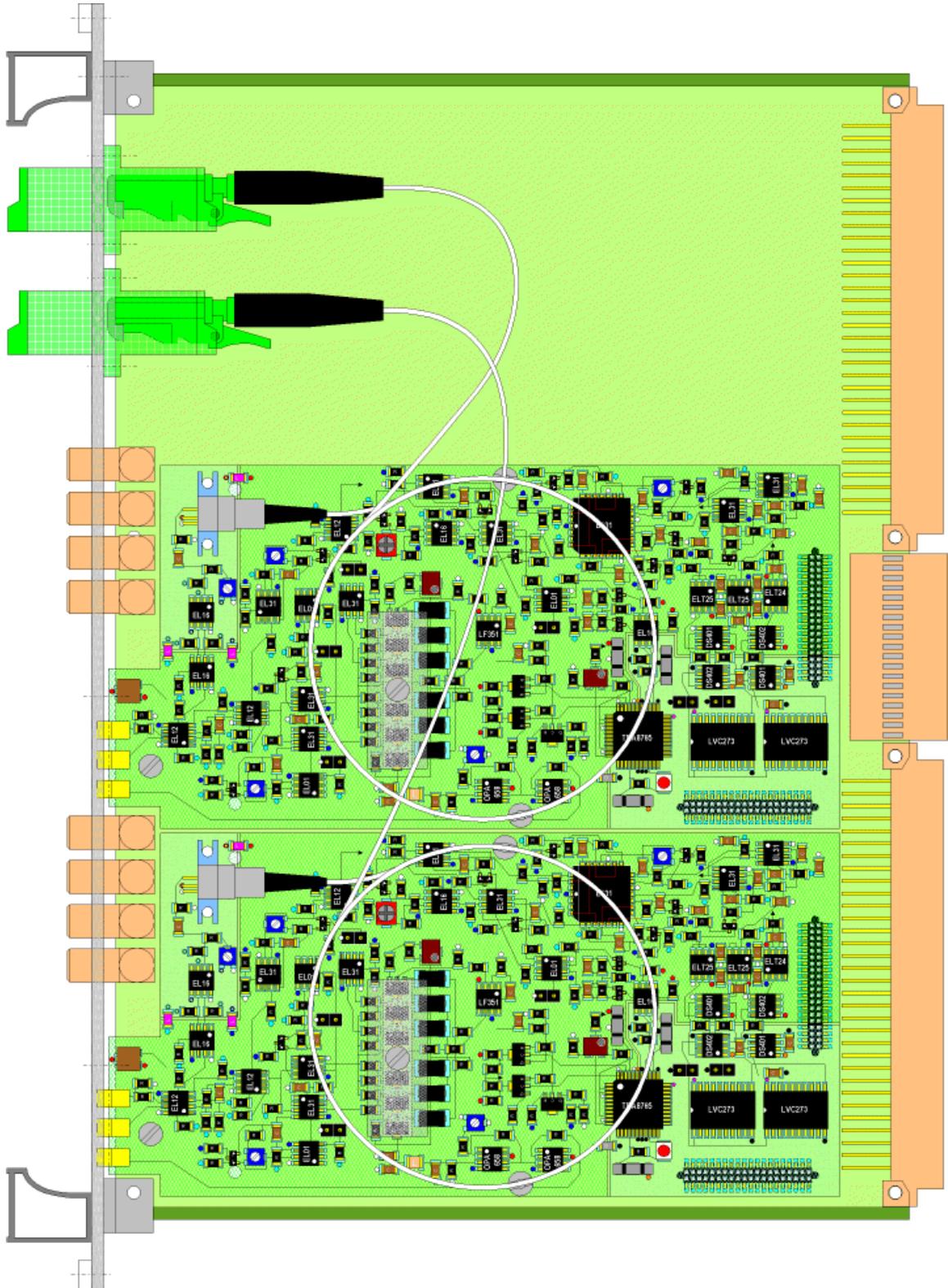


Figure B1: Overall layout of the WBTN mezzanine cards.

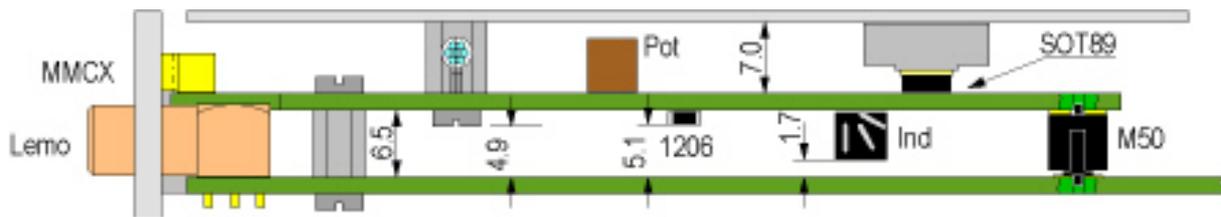
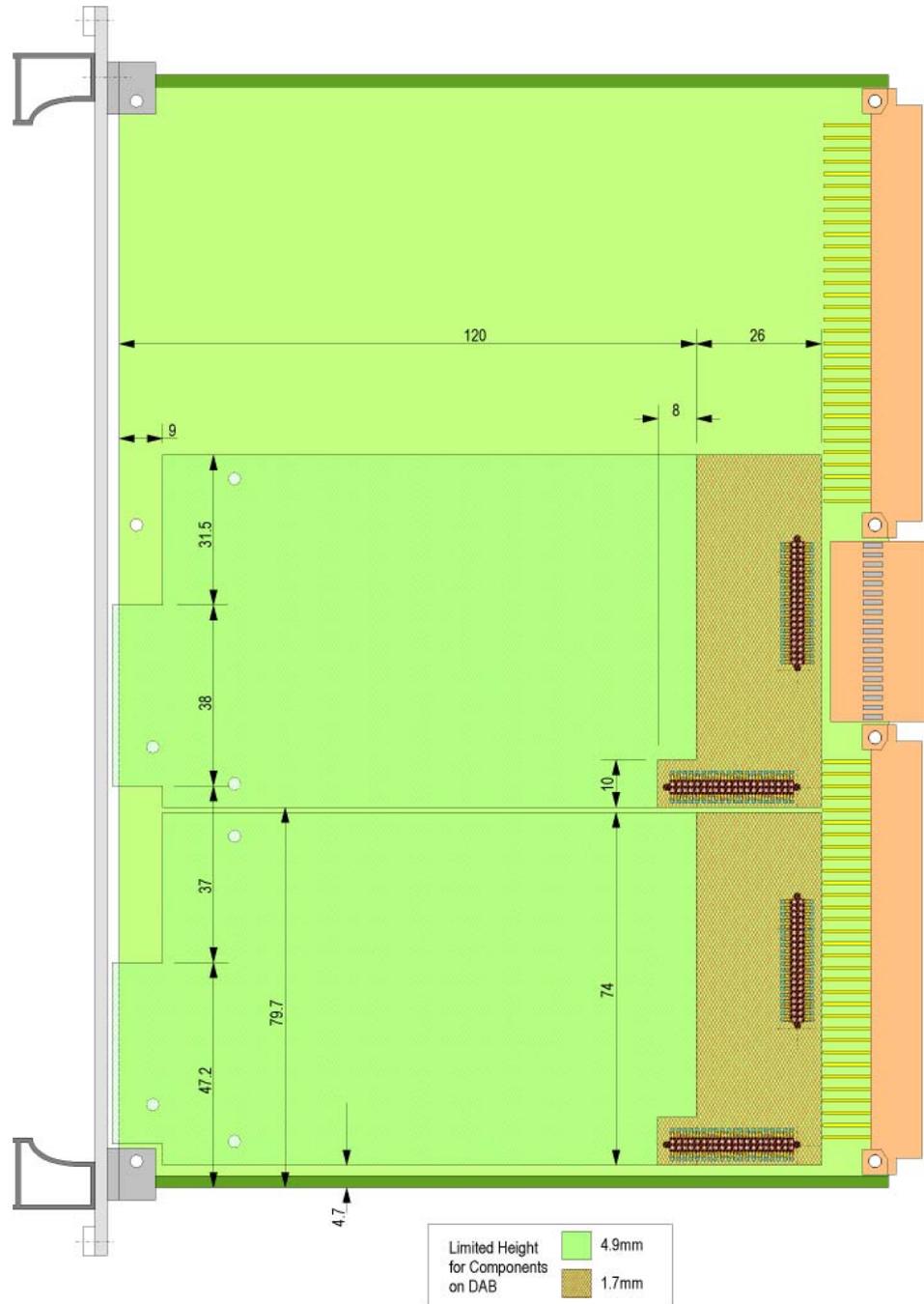


Figure B2: Mezzanine card dimensions and zones of limited height.

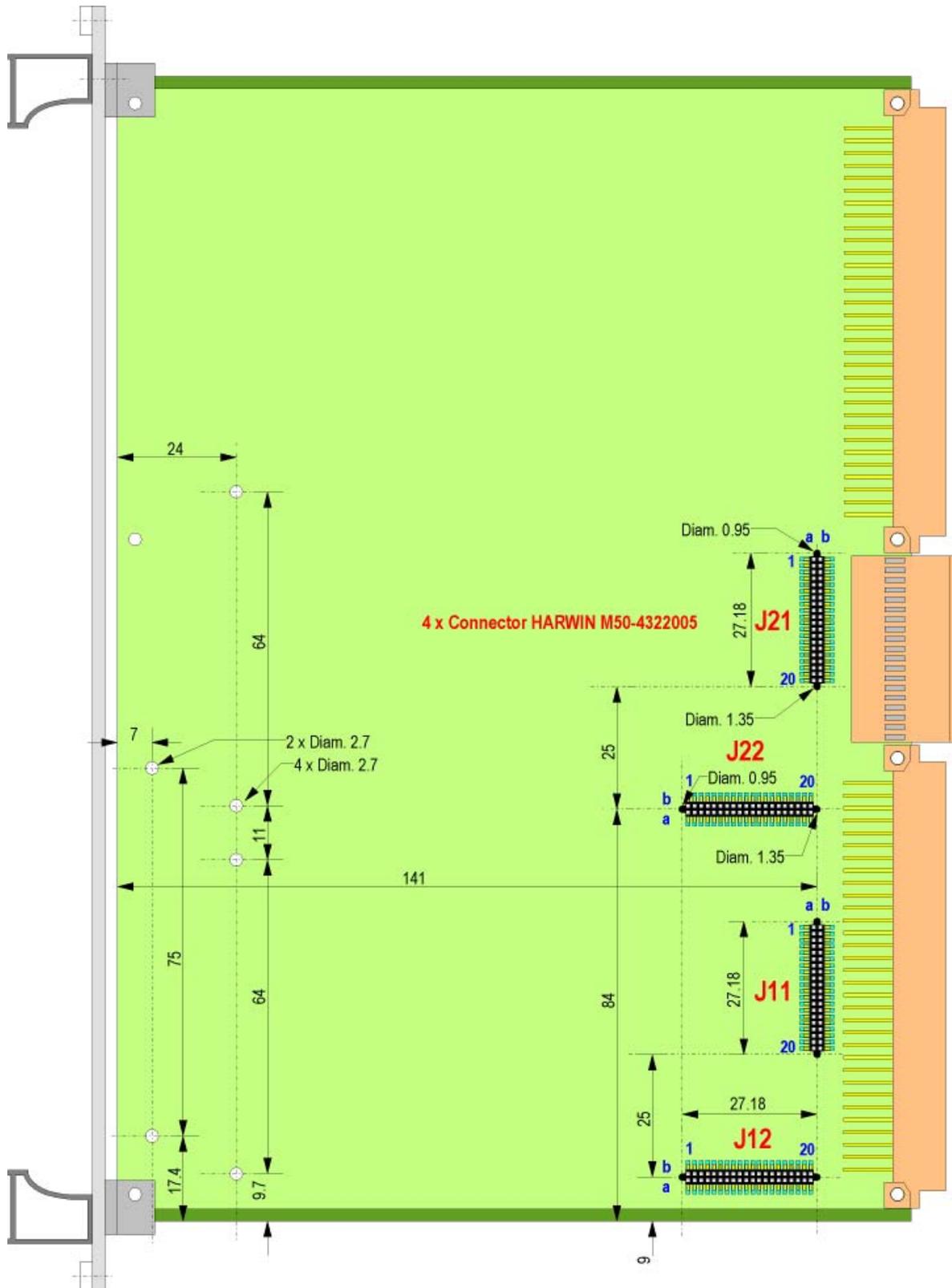


Figure B3: Mezzanine connector positions.

