

V233

FUNCTION GENERATOR

FUNCTIONAL DESCRIPTION

3/17/08

Written by Charles R. Theisen

TABLE OF CONTENTS

Associated Drawings.....	Page 1
Overview.....	Page 2
Timing Triggers Instead Of Setpoints.....	Page 4
PSI Communications.....	Page 6
Timing Examples Of PSI Communications.....	Page 7
Setpoint And Readback Buffers.....	Page 9
Setpoint Bit Mapping.....	Page 10
Readback Bit Mapping.....	Page 12
How A Function Is Sent.....	Page 13
How A Single Frame Is Sent.....	Page 18
Front Panel Layout.....	Page 22
Front Panel LED Indicators.....	Page 23
Front Panel Connectors.....	Page 24
Backplane Connectors.....	Page 25
VME Interface.....	Page 26
Board Identification.....	Page 28
Event Link Decoding.....	Page 29
Event Link Simulator.....	Page 31
PPM Operation.....	Page 32
Addressing Setpoint And Readback Buffers.....	Page 34
Start And Resume Delay Memory.....	Page 38
Clock Select Register.....	Page 39
Frame ID Register.....	Page 41
Start Event Register.....	Page 42
Resume Event Registers.....	Page 43
Group End Event Register.....	Page 44
Single Cycle Operation.....	Page 45
Tag Event Register.....	Page 46
Arming Channels.....	Page 47
Setpoint Count Registers.....	Page 48
Switching Readback And Setpoint Buffers.....	Page 49
Sending VME Commands.....	Page 53
Interrupts And Status.....	Page 54
Missing Readback Count Registers.....	Page 63
Board And Channel Resets.....	Page 64
Grounding Jumpers.....	Page 67
Revisions.....	Page 68
Appendix A.....	V233 Register Assignments
Appendix B.....	V233 Register And Memory Descriptions
Appendix C.....	V233 Programming Instructions
Appendix D.....	V233 Test Procedure

V233 Function Generator

ASSOCIATED DRAWINGS

CA3010010 V233 Schematic Diagram
CA3010011 V233 Drill Detail
CA3010012 V233 PCB Assembly
CA3010013 V233 Front Panel Detail
CA3010014 V233 Module Assembly
CA3010042 V233 Programmed Assembly

OVERVIEW

The V233 Function Generator Module is packaged as a standard 6U VME board. The V233 module is to control and retrieve status from as many as 4 power supplies. In its normal configuration, a V233 communicates directly with up to 4 PSIs, (Power Supply Interfaces), which in turn are used to interface to the power supplies. The V233 sends serially formatted command, setpoint (voltage reference), and read frames to the PSI over a fiber optic link operating at 50MHz. The PSI decodes the frames, and translates them to provide the necessary control signals and voltage references to the power supply. The V233 also receives power supply status and readbacks via the PSI on a separate fiber optic input, also operating at 50MHz.

The primary function of the V233 is to send a continuous series of setpoint frames, called functions, to the PSI. However, individual power supply commands, such as On, Off, and Standby, can be sent via the V233. Each time a command is sent, the power supply status is retrieved. Commands may be sent anytime a function is not being generated.

Setpoints, which are loaded into the V233's on-board memory by an operator, are output at a pre-selected rate in order to precisely control a power supply's output. Each setpoint sent to a power supply normally results in a corresponding set of 6 readback words. (This depends on the Frame ID sent with the setpoint) The readbacks from the power supply are also stored in on-board memory, and made available for retrieval after the function is finished. The V233 uses 2 sets of buffers for setpoints and readbacks. While one function is being generated, a new function can be loaded.

Setpoints may be sent at 100Hz, 1KHz, 10KHz, or 100KHz. If desired, there is an external clock input that can be used to clock out the setpoints. Unlike the V133 module, which cannot retrieve readbacks in the 100KHz mode, the V233 can get readbacks at 100KHz, because it operates with a PSI link speed of 50MHz. At 1MHz option is also available, but is not used for normal operations. No readbacks can be retrieved at this rate.

Once setpoints are stored in memory, the function can be started by an event on the Event Link, a VME command, or an external pulse. Delays of up to 16 seconds may be applied to the start of a function.

Programmed pauses can be included in a function. While paused, the V233 continually transmits the last setpoint so that readbacks are still received. A paused function can be resumed by an event on the Event Link, a VME command, or an external pulse.

When the last setpoint of a function is retrieved from memory, it is continually re-transmitted to the PSI until a pre-defined Group End event occurs. During this time, readbacks are still being received and stored. The occurrence of Group End halts all PSI communications.

V233 Function Generator

The V233 has 4 separate output channels, providing control for as many as 4 power supplies. Each channel has 1 fiber optic transmitter and receiver. Channels are operated and configured independently, allowing for different start and resume events, function lengths, and transmission rates. In addition, the V233 module is PPM capable, with provisions for as many as 8 individual users, each one capable of generating a unique function.

Control of the V233 module is accomplished by programming various on-board registers. Some registers are for board level operations, such as Event Link decoding, PPM control, etc. In addition, each channel has its own set of dedicated registers, which allow independent control and operation of the 4 channels.

TIMING TRIGGERS INSTEAD OF SETPOINTS

Each V233 has 4 channels of fiber optic I/O. Each channel is normally used to send functions, comprised of setpoints stored in memory, to a power supply. Each setpoint is a 16-bit value representing a voltage between -10 and +10 volts.

As the channel 1 and channel 2 setpoints are sent out, each 16-bit value is also latched and presented in a parallel fashion on the VME P2 connector. These are the Timing Trigger outputs of the channels. Instead of loading the on-board memory of channel 1 and 2 with setpoints, consecutive binary values, called timing tables, can be loaded. These timing tables will create timed pulses, available as separate channels on the VME backplane. Each bit place in memory represents a timing trigger channel. Two channels can combine to generate up to 32 channels of timing triggers. If a channel is used for timing triggers, the fiber optic output of that channel cannot be connected to a PSI. However, the channel is controlled using the same registers as if setpoints were being generated.

Normally, timing tables consist of binary 0's. Pulses are created by loading binary 1's into pre-determined bit positions. The selected setpoint clock determines the resolution of the timing triggers. Using the 100KHz clock, pulses with a 10us resolution can be constructed. Programming consecutive memory locations with a binary 1 programmed into the same bit position will produce a 20us pulse. Alternating 1's and 0's can simulate a finite pulse train of 50KHz.

The advantage of generating timing signals using this method is that the pulses are synchronized with the functions being generated by other V233s. Every V233 channel, whether it is used for setpoints or timing triggers, can be synchronized to start transmitting its data at the same time, through the use of a common event. Furthermore, each channel clocks out its data with a common clock derived from the same Event Link. When users are changed or tables are swapped, the synchronization between V233s remains constant.

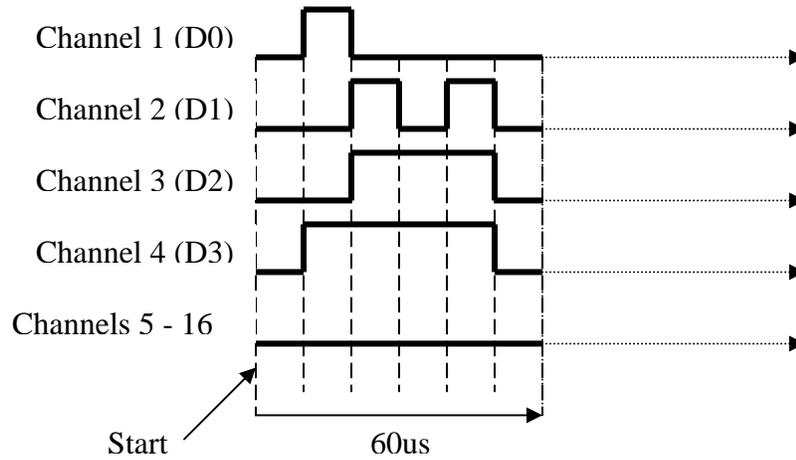
Below is an example how to use a channel's timing trigger table in a V233 to generate 16 channels of timing triggers. Bit column D0 of memory translates to Timing Trigger Channel 1, the D1 column is Channel 2, and so on. A small section of programmed memory and the resultant timing trigger channels are shown. A setpoint clock of 100KHz is assumed.

V233 Function Generator

V233 Timing Trigger Table

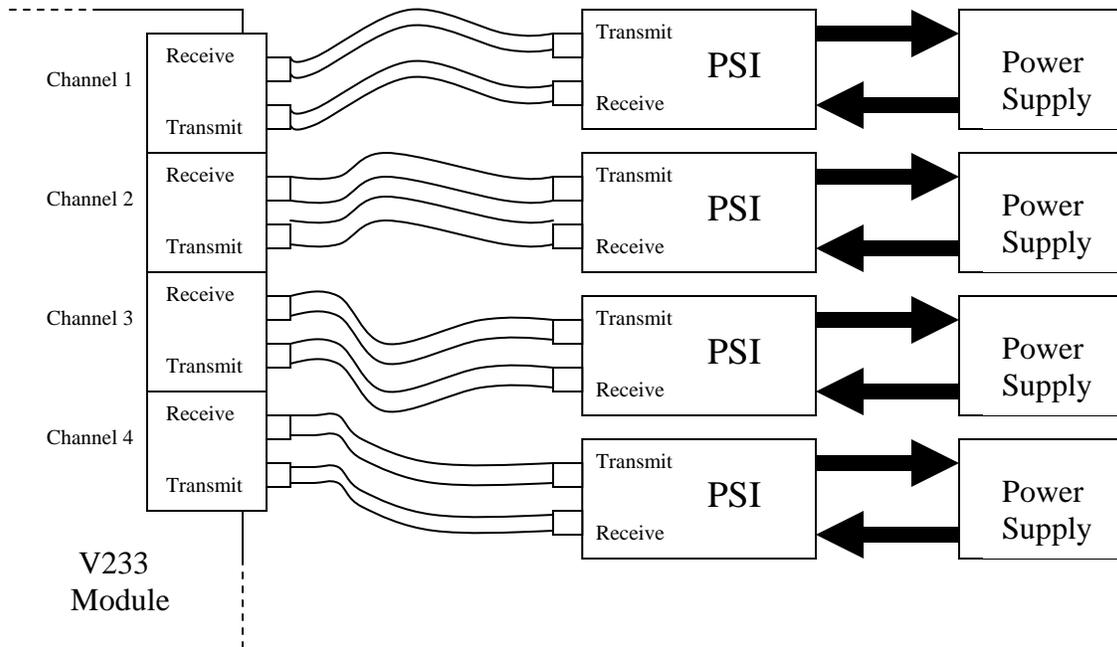
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address 0
0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1	Address 1
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	Address 2
0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	Address 3
0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	Address 4
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Address 5

Resultant Timing Triggers



PSI COMMUNICATIONS

The following is a brief discussion of the communication between the V233 and a PSI. It is not intended to be a technical description or specification of a PSI.

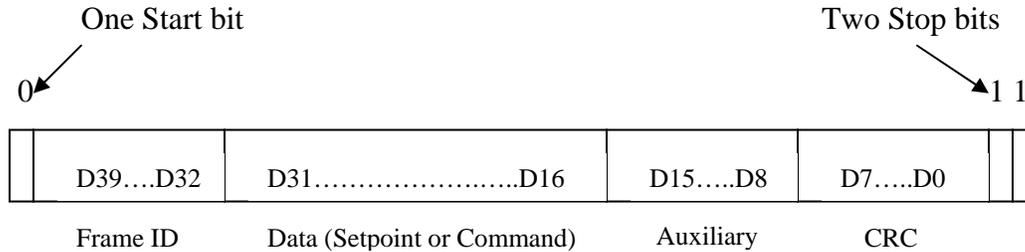


It is important to remember that in the Function Generator's default state, most internal clocks are derived from the Event Link. Therefore, unless an operational Event Link is connected to the V233, the PSI interface will not work. An on-board oscillator can be used to provide these internal clocks if desired, providing each channel's Clock Select register is programmed properly. However, this removes a level of synchronization and repeatability that the board normally provides.

Each channel of the V233 has both fiber optic transmitter and receiver circuitry. These serial links to and from the PSI are Manchester encoded, and operate at 50MHz. The links are always active, with idle periods consisting of 1's continually sent to and received from the PSI. When a channel's fiber optic transmit output is connected to the fiber optic receive input of a PSI, the PSI's "LINK" light should be constantly on. When the fiber optic transmit output of an idle PSI is connected to a channel's fiber optic receive input, that channel's Receive LED ("R1", "R2", "R3", or "R4") should flash once every 2 seconds. When the PSI is sending readbacks to the Function Generator, every decoded word will cause the channel's Receive LED to flash. When a function is being transmitted, readbacks are received so fast that Receive LED will be constantly on.

V233 Function Generator

During the transmission of a function, setpoints are transmitted to the PSI, and readbacks are received from the PSI. All PSI words, setpoints, readbacks, and commands, are encoded into 43 bit frames as shown below.



Every word begins with 1 Start bit, set to zero, followed immediately by an 8-bit Frame ID, a 16-bit Data field (containing the setpoint or command), 8 Auxiliary bits (formerly Reserved bits), an 8-bit CRC, and 2 Stop bits.

The CRC is generated using the polynomial $(x^8 + x^7 + x^5 + x^4 + x + 1)$, but it excludes the start (0) bit and two stop (11) bits.

The Frame ID determines the response from the PSI. Unlike the V133, where the Frame ID is fixed, the V233 has a programmable Frame ID. It is the responsibility of the operator to ensure a proper Frame ID is used, normally 15h, that will result in 6 readback words returned by the PSI in response to a setpoint. The readbacks are shown below.

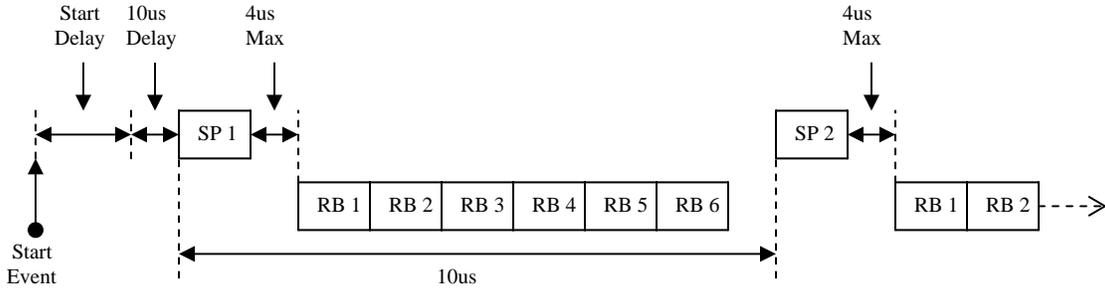
- 1) Echo
- 2) Status
- 3) ADC1
- 4) ADC2
- 5) ADC3
- 6) ADC4

It takes .86 microseconds (us) to transmit a word over the fiber optic link to the PSI. A PSI is allowed a maximum of just under 4us to begin its response. Since the PSI will respond with 6 words, total transmission time for sending a setpoint and acquiring the readbacks will be a maximum of 10us. Since a 100KHz clock has a period of 10us, this is the fastest rate that setpoints can be sent to a PSI when expecting readbacks.

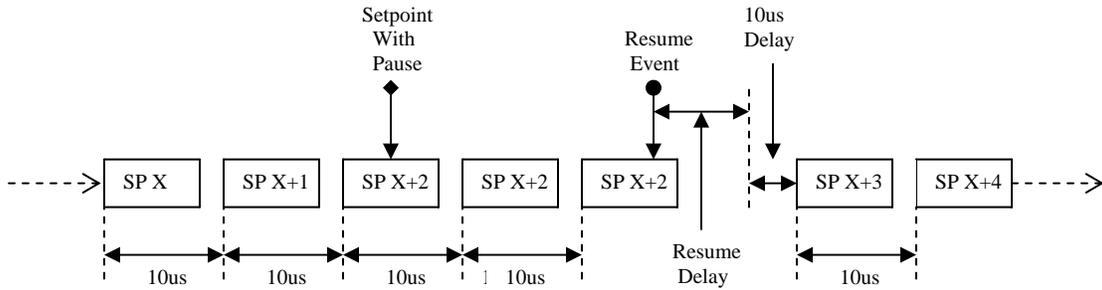
In addition to the normal mode of sending functions, the V233 module can be used to send individual command or read frames to the PSI. The Frame ID is set to an appropriate value, and the 16-bit data field contains the command. This utility will be covered later in this document.

TIMING EXAMPLES OF PSI COMMUNICATIONS

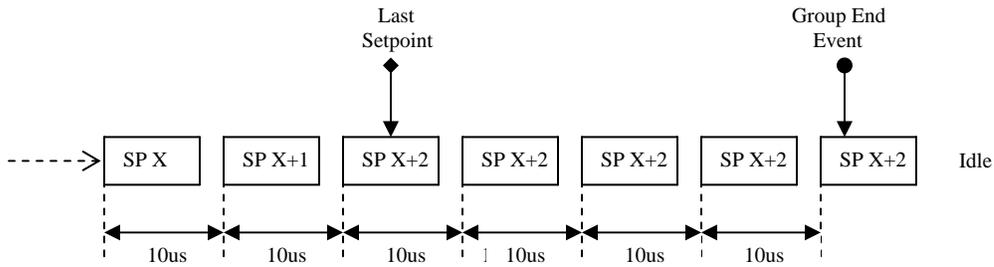
Function Start Using 100KHz Clock (Readbacks Shown)



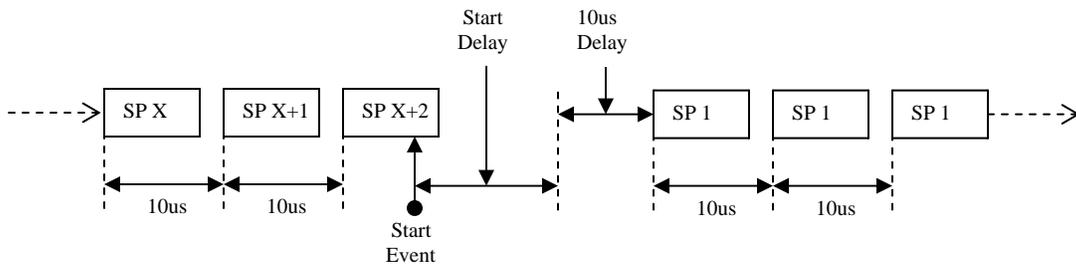
Function Resume Using 100KHz Clock (Readbacks Not Shown)



Function End Using 100KHz Clock (Readbacks Not Shown)



Re-Started Function Using 100KHz Clock (Readbacks Not Shown)



SETPOINT AND READBACK BUFFERS

All setpoints and readbacks are stored in on-board dynamic random access memory (DRAM). The VME controller can read and write to this memory using A32/D32 data transfers only. The actual memory components used are manufactured by Micron, part number MT48LC32M16A2TG-75, which is essentially a 32M x 16 device. Each channel utilizes 2 of these devices in parallel, providing a 32-bit wide data path. All hand shaking signals for these memory devices, including memory refresh, are handled by the channel gate arrays.

Each channel's DRAM is divided into separate setpoint and readback buffer areas. Two individual setpoint buffers are reserved for each of the 8 possible users, resulting in a total of 16 setpoint buffers per channel. One user setpoint buffer can hold 1,048,576 setpoints. Each user always has one active setpoint buffer, and one inactive setpoint buffer. Once the channel is armed and a Start event occurs, the appropriate user's active setpoint buffer supplies the setpoints necessary for generating a function. While a user's active setpoint buffer is generating a function, the user's inactive buffer can be loaded with a new function. If users are changed, halting the ongoing function, the next Start event will begin a new function, with the new user's active buffer supplying the setpoints.

If commanded, the occurrence of the Group End event will cause the user's active and inactive setpoint buffers to switch, permitting the generation of new function for the same user. It is not necessary for all users to have their setpoint buffers switched from active to inactive, and visa versa, at the same Group End event.

It is important to note that a user may not 'borrow' setpoint memory from other users. The 1 meg boundary is fixed. Even if PPM is not used, the limit is still 1,048,576 setpoints for a function, because in non-PPM mode it is the user 1 buffers that are used for setpoint storage. However, using a setpoint clock of 100KHz, a 1 meg user setpoint buffer can produce a function over 10 seconds long, not including pauses.
(1,048,576 setpoints / 100,000 setpoints per second = 10.48576 seconds)

Readbacks also require 2 sets of buffers. As with the setpoint buffers, there is an active readback buffer and an inactive readback buffer. However, unlike the setpoint buffers, the readback buffers are not partitioned into individual user buffers. Each readback buffer can hold up to 8,388,608 (8 meg) readbacks. At 100KHz, this provides storage for about 14 seconds worth of readbacks, from the time the first function is started to a Group End event. (8,388,608 readbacks / 600,000 readbacks per second = 13.981 seconds) During the generation of 1 or more user functions, 1 readback buffer is active in order to provide readback storage. Unlike the setpoint buffers, which only switch at Group End when commanded, the readback buffers are switched upon every Group End event. After switching, the newly activated readback buffer is available to store the readbacks of the next user function. The deactivated readback buffer holds the readbacks from the previous user functions. This buffer is now available to be read by the VME controller. The readbacks in the deactivated readback buffer must be read prior to the next Group End event, when the readback buffers are switched yet again.

V233 Function Generator

If any one of the overhead bits D20 through D16 is set, it indicates that the function has reached a pause. The setpoint value included in this word, (D15 – D0), will be repeatedly sent by the Function Generator until the Resume event associated with the active pause bit occurs. Each pause bit can have only 1 Resume event associated with it. Since there are 5 pause bits, there can be 5 different events chosen to resume a paused function. A function can be paused multiple times. If desired, the same pause bit can be used more than once during a function.

Pause bits D19 through D16 are associated with programmer specified Event Link words. When a function is paused by bit D16 being set, only the Event Link word assigned to that pause bit will cause the function to resume. The specific Event Link words used for resuming a function are determined by programming specific gate array registers, which will be described in detail later in this document.

When bit D20 is set, the only way to resume the function is to send a VME Resume command. A VME Resume command is issued by setting bit D1 of a channel's VME Commands register, also described later in this document.

If 2 or more setpoint overhead bits are inadvertently set in the same word, only 1 will be recognized. The order of precedence is D31, followed by D16, D17, D18, D19, and D20.

REDABACK BIT MAPPING

When readbacks are stored in the readback buffers, they are formatted as shown below.

REDABACK BIT-MAP																												
M																												L
S																												S
B																												B
D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D	D
3	3	2	2	2	2	2	2	2	2	2	1	1	1	1	1	1	1	1	1	1	9	8	7	6	5	4	3	2
1	0	9	8	7	6	5	4	3	2	1	0	9	8	7	6	5	4	3	2	1	0							0
S	P	E	U	U	U	E	C	I	I	I	I	I	I	I	R	R	R	R	R	R	R	R	R	R	R	R	R	R
T	A	N	S	S	S	O	R	D	D	D	D	D	D	D	E	E	E	E	E	E	E	E	E	E	E	E	E	E
A	U	D	E	E	E	T	C								A	A	A	A	A	A	A	A	A	A	A	A	A	A
R	S		R	R	R	/		7	6	5	4	3	2	1	0	D	D	D	D	D	D	D	D	D	D	D	D	D
T	E	F				T	E								B	B	B	B	B	B	B	B	B	B	B	B	B	B
		U	C	C	C	A	R								A	A	A	A	A	A	A	A	A	A	A	A	A	A
F	F	N	O	O	O	G	R								C	C	C	C	C	C	C	C	C	C	C	C	C	C
U	U	C	D	D	D	O									K	K	K	K	K	K	K	K	K	K	K	K	K	K
N	N	T	E	E	E	R																						
C	C	I													M													
T	T	O	M		L										S													
I	I	N	S		S										B													
O	O		B		B																							
N	N																											
* User Code: 000 = User 1, 001 = User 2,...111 = User 8																												
** When D25 is set for EOT, (End Of Table), all other bits are zero																												

The lower 24 bits are made up of the Frame ID and the Data Field that are in every word sent by the PSI (readbacks) in response to a setpoint. The upper 8 bits are overhead bits. As established earlier, there are 6 Readbacks words returned for every setpoint sent. The state of the readback overhead bits, with the possible exception of the CRC Error bit, will be the same for all 6 words. The readback overhead bits are defined as follows:

- D31: Start Function...If set, indicates readback is associated with the first setpoint of a function.
- D30: Pause Function...If set, indicates readback has been acquired while a function is paused.
- D29: End Function...If set, indicates readback is associated with the last setpoint of a function, and beyond, until Group End occurs.
- D28 -> D26: User Code...Indicates which user was operational when setpoint was sent.
000 = User 1, 001 = User 2, 010 = User 3, 011 = User 4,
100 = User 5, 101 = User 6, 110 = User 7, and 111 = User 8.
- D25: EOT/TAG. If set for End of Table, indicates the end of the current readback table, and all other data bits in the word are zero.
If set for a TAG, other bits contain normal values.
- D24: CRC Error...If set, indicates readback was received with a CRC error. If bit is set in an echo readback, PSI may have received setpoint with CRC error, because the 50MHz PSI echoes the CRC as well as the setpoint.

HOW A FUNCTION IS SENT

A function is built for each user by loading setpoints into the individual user setpoint buffers. The PSI responds to each setpoint sent to it with 6 readback words, which the V233 stores in its readback buffers. The setpoint and readback buffers are located in on-board DRAM. Each channel of the V233 module has 2 readback buffers. Each channel also has 16 available setpoint buffers, 2 for each possible user. While one readback buffer is active, the other readback buffer is inactive. Similarly, each user has 1 active setpoint buffer, and 1 inactive setpoint buffer. If PPM is not used, only the user 1 setpoint buffers and registers require programming.

The following steps must be taken to start sending a function to a PSI. The order is not critical, except that arming a channel should always be the last step taken. All registers are described in detail later in this document.

- 1) Program User Switch Code register (Set to 0000h if PPM not used)
- 2) Program User Code registers (If PPM used)
- 3) Program channel's Start Event register
- 4) Program channel's Start Delay registers
- 5) Program channel's Resume Event registers (If required)
- 6) Program channel's Resume Delay registers (If required)
- 7) Program channel's Group End event register
- 8) Program channel's Clock register (Select setpoint clock)
- 9) Program channel's Frame ID register
- 10) Load setpoints into channel's active setpoint buffers
- 11) Program Channel Arm register to arm channel

When the V233 is first powered, all setpoint and readback buffers contain meaningless values, and all 4 channels are disarmed. The module defaults to user 1, but if PPM is used and the user registers are programmed, the appropriate user will become operational when dictated by events on the Event Link. The first function for each user must actually be loaded into the user's **active** setpoint buffers, the "1" buffers, but prior to arming the channel. This is the only time active setpoint buffers can and should be written. The V233 will not allow writing to active setpoint buffers once the channel is armed. All subsequent functions must be loaded into inactive buffers, unless the channel is disarmed.

A function is loaded into a user's setpoint buffer starting with the first address of the buffer, and continues in consecutive addresses until the last setpoint is reached. Once all the user setpoints have been loaded and the channel is armed, a function can be started in 3 possible ways. The primary method used to start a function is the occurrence of the channel's Start event on the Event Link. However, an external Start pulse or a VME Start command can also be used to start a function. The Start Event, external Start pulse, and VME Start command are essentially ORed together. Unlike the VME Start command, which can be issued any time, the Start Event and the external Start pulse must be enabled prior to being used. The external Start pulse and VME Start command are discussed in more detail later in this document.

V233 Function Generator

Every user of every channel has a programmable 24-bit start delay associated with the start of their function. The start delays are stored in Dual Port RAM, internal to each channel's FPGA. When a Start event or an external Start pulse occurs, the appropriate start delay is loaded into a 24-bit down counter. The counter is clocked by a 1MHz clock, which is re-synchronized upon every occurrence of a Start event or Start pulse. The start delay can range from zero, represented by a value of 000000h, to 16.777215 seconds, represented by a value of FFFFFFFh. If a VME Start command is used to start a function, the programmable start delay is forced to zero, regardless of the user or the value of the delay stored in RAM.

The programmable start delay begins to count down as soon as the Start event or Start pulse occurs. Immediately following the programmable start delay, a fixed delay of 10us is added for the 100Hz, 1KHz, 10KHz, or 100KHz setpoint clocks. If the 1MHz setpoint clock is selected, the fixed delay is 1us. These delays cannot be removed by the operator. The 10us delay ensures that a PSI would have enough time to send readbacks in response to any setpoint received just prior to the occurrence of a subsequent Start event, external Start pulse, or VME Start command. The 1us delay, used only with the 1MHz setpoint clock, is the minimum time needed by a PSI to receive and process a setpoint. At 1MHz, there is no time allotted for readbacks. For this reason, the 1MHz setpoint clock cannot be used for normal operation.

Setpoints are never sent to the PSI during the programmable start delay, or the built-in 10us or 1us delay. In fact the channel's setpoint clock is turned off during these delays.

At the end of the fixed delay, the channel's selected setpoint clock is started, and the function's first setpoint, found at the first address of the user's active setpoint buffer, will be retrieved, encoded, and sent to the PSI. After that, each positive going edge of the setpoint clock will cause the next setpoint in the user's active setpoint buffer to be retrieved, encoded, and sent to the PSI.

Assuming the correct Frame Id is sent with every setpoint, 6 readback words will be sent back to the V233 from the PSI. These readbacks are automatically stored in the channel's active readback buffer, starting at the first address of the buffer, and continues on sequentially until a Group End event, an external Group End pulse, a VME Group End command occurs, or until the active readback buffer is full. Once an active readback buffer is full, subsequent readbacks will be lost. Readbacks will continue to be lost until the active and inactive readback buffers are swapped by a Group End occurrence, or until the channel or module is reset.

If a setpoint word contains an active pause bit, that setpoint will be repeated at the channel's setpoint clock rate until the function is resumed. A function is resumed after the appropriate Resume event, external Resume pulse, or VME Resume command occurs, and only after the appropriate resume delay expires. The resume delay always includes a built-in delay of 10us added to the end of the programmable resume delay.

V233 Function Generator

Every user of every channel has a 24-bit programmable resume delay for each of the 4 possible Event Link Resume events. (Resume 1 event, Resume 2 event, Resume 3 event, and Resume 4 event). Like the start delays, the resume delays are stored in internal Dual Port RAM, and when the appropriate Resume event occurs, its associated resume delay value is loaded into the same 24-bit down counter used to generate the start delay. The resume delay ranges are the same as the start delay range.

An external Resume pulse and a VME Resume command are also available for use. When an external Resume pulse is used, it is always applied as a Resume 1 event, and always uses the Resume 1 delay. The Resume 1 Event and external Resume pulse are essentially ORed together. All 4 Event Link Resume events as well as the external Resume pulse must be enabled prior to being used. The VME Resume command can be issued at any time, but will only work if a function is in a VME pause. The external Resume pulse and VME Resume command are discussed in more detail later in this document

The programmable resume delay begins as soon as the Resume event or external Resume pulse occurs. When a VME Resume command is used to resume a function, the programmable resume delay is forced to zero, regardless of the user. Immediately following the programmable resume delay, a built-in delay of 10 μ s is added. This delay is fixed, and cannot be removed by the programmer. It is there to make sure there is always a minimum delay of 10 μ s prior to actually sending the next setpoint to the PSI following a pause. The setpoint that initiated the pause is continually sent to the PSI during the pause and during the programmable resume delay, but not during the built-in 10 μ s delay. In fact the channel's setpoint clock is turned off during this time. At the end of the built-in 10 μ s delay the setpoint clock is re-started. The next setpoint in the user's active setpoint buffer is retrieved, encoded, and sent to the PSI. After that, each positive going edge of the channel's setpoint clock will cause the next setpoint in the user's buffer to be retrieved, encoded, and sent to the PSI.

Once the last setpoint has been taken from the setpoint buffer and sent to the PSI, it will be repeated at the setpoint clock rate until there is a Group End event, an external Group End Pulse, or a VME Group End Command, which are essentially ORed together. Unlike the VME Group End command, which can be issued any time, the Group End Event and the external Group End pulse must be enabled prior to being used. The external Group End pulse and VME Group End command are discussed in more detail later in this document.

When a Group End event, external Group End pulse, or VME Group End command occurs, setpoint transmissions to the PSI are halted. Readbacks are halted as well, even if a PSI is still responding to the last setpoint. This means the last setpoint sent to the PSI may not have all of its corresponding readbacks stored in the readback buffer. In fact, depending when Group End occurred in relation to when the last setpoint was received by the PSI, none of the readbacks for the last setpoint may be stored.

V233 Function Generator

Once setpoints are halted, the fiber optic link to the PSI will go into an idle condition, which consists of a continual string of Manchester encoded binary 1's. The PSI fiber optic link will remain idle until another function is started. There are 3 possible ways to start another function:

- 1) The same user function is re-started by another Start event
- 2) The user's active setpoint buffer was switched at Group End, and a new function for the same user is started by another Start event.
- 3) The user changes, and a new user function is started by another Start event.

Besides halting setpoints and readbacks, the occurrence of Group End has several other purposes. It writes the value 02000000h into the next available address of the channel's active readback buffer, which immediately follows the last stored readback. It then resets the readback buffer address. It causes each pre-selected user to swap their active and inactive setpoint buffers. It also causes the channel's active readback buffer to become inactive, and activates the previously inactive readback buffer. This switching of readback buffers occurs even when the channel is dis-armed.

Each channel has a 24-bit setpoint counter, which keeps track of the number of setpoints sent to the PSI. The count begins with the first Start event after arming the channel or after a Group End event, and ends when the next Group End event occurs. Upon Group End, the count is latched into the channel's Setpoint Count High register and the Setpoint Count Low register. Then the setpoint counter is cleared. The next Start event will re-start the setpoint counter. This process ensures that the Setpoint Count High register and the Setpoint Count Low register are only updated upon the occurrence of a Group End event.

As already established, when Group End occurs, setpoint transmission is ended. Normally, the next occurrence of a Start event will begin another function. However, it is possible to instruct a channel to halt all new functions upon the occurrence of Group End. This is accomplished by setting bit D9 of the channel's Group End Event register. If D9 is set when Group End occurs, including the external Group End pulse or the VME Group End command, the channel goes into a halt state. However, this mechanism only works after a function has been started. If no function was started before the occurrence of a Group End event, the channel will not be halted. The first Start event will still begin the function, and then the next Group End event will halt the channel. A halted channel is indicated by the V233 setting bit D10 of the channel's Group End Event register. When D10 is set, another function cannot be started. Once D10 is cleared, the next Start event will start the new function. If D9 remains set, the next Group End will again halt the channel.

V233 Function Generator

Group End is not the only thing that can halt setpoint transmission. Setpoints will also be ended by the following occurrences:

1. Another Start event, external Start pulse, or VME Start command.
2. Issuing a channel or board reset.
3. Dis-arming the channel.
4. A user change, if using PPM mode.

Like a Start event, changing users causes the channel's setpoint buffer address generator to be reset, but it does not reset the channel's readback buffer address generator. When a user change occurs, any ongoing setpoint transmissions from the previous user's function are halted, and the channel waits for a new Start event. If desired, the Event Link word used to switch users can also be used as the Start event. Once the new user is operational and a Start event occurs, the new user's start delay and the built-in 10 μ s delay are counted down. Once the start delay is finished, the first setpoint of the new user's function is sent. Readbacks for the new user function continue to be stored in the active readback buffer, starting immediately after the last readback that was stored for the previous user.

If a user function is ended prematurely for any reason, such as a Group End event, another Start event, a reset, dis-arming the channel, or a user change, a large step change in the output state of the power supply may occur when the next function is started. The programmer should make sure that the length of a user function does not exceed the expected time between any of these occurrences. If it does, individual setpoints may have to be sent to the PSI in order to "walk down" the output of the power supply prior to allowing a new function to start.

HOW A SINGLE FRAME IS SENT

The V233 provides a utility to send an individual command, setpoint, or read frame to a PSI. Command examples are Off, On, and Standby. These individual frames are separate from a normally transmitted function, and are not associated in any way with the setpoint buffers and readback buffers located in the on-board DRAM.

Individual frames may be sent at any time while a channel is dis-armed. If a channel is armed, the Function Generator can be instructed to automatically send a frame as soon as the channel is dis-armed. The Function Generator can also be instructed to automatically send a frame 10us after the occurrence of a Group End event. The 10us delay is fixed, and the frame will be sent whether the channel is armed or not. This is useful for sending commands to a power supply immediately following the end of a function.

Each channel has its own set of registers reserved for the single frame utility. These registers are accessed using A24/D16 or A24/D08(EO) data transfers.

Each channel has 2 registers that must be programmed prior to sending a frame. They are described below. The location of these registers may be found in Appendix A and Appendix B.

Ch X Single Frame ID Register

This is a 16-bit register that may be written as well as read. Its contents make up the Frame ID and the Auxiliary bits of the PSI word.

D15 through D8 are the Auxiliary bits. Currently, PSIs only use the Auxiliary bits found in setpoint words, not in commands.

D7 through D0 make up the Frame ID, which essentially determines the type of frame (command, setpoint, or read) being sent to the PSI.

The PSI currently recognizes the following Frame Ids:

55H = Setpoint without read
15H = Setpoint with read
4AH = Command without read
0AH = Command with read
00H = Read Command
40H = Read Status/ADC

Ch X Single Frame Data Field Register

This is a 16-bit read/write register that holds the PSI word's data field value. Consult the power supply's documentation to determine the required values.

V233 Function Generator

Once the Single Frame ID register and the Single Frame Data Field register are programmed, the frame may be sent to the PSI. To initiate transmission of the frame, use the Ch X Send Single Frame register, described below.

Ch X Send Single Frame Register

This is an 8-bit read/write register. The register is automatically cleared after a command is sent. D0, D1, and D2 are the only meaningful bits. D3 -> D7 are not used.

D0 – When set, instructs the V233 to send the frame when the channel is not armed. If the channel is armed and D0 is set, the frame will be sent as soon as the channel is dis-armed.

D1 - When set, instructs the V233 to send the frame when a Group End event occurs, whether the channel is armed or not. There is a built-in delay of 100us from the time the Group End event is received to the time the frame is actually sent.

Note: Both D0 and D1 may be set simultaneously. If so, the frame will be sent when either of the frame transmission requirements is satisfied. The register is then cleared immediately, and all bits are reset.

D2 - D2 inhibits the Timing Trigger update. If bit D2 is set, the channel will not send the data field of the single frame to the 16-bit parallel Timing Trigger output. Instead, it will maintain the previously converted value. This is especially important if using channel 1 and channel 2 of the V233 to generate timing triggers instead of setpoints.

Any readbacks resulting from a transmitted command will be stored sequentially in the channel registers described below.

Ch X Readback ID 1 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 1st readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored.

Ch X Readback Data 1 Register

This is a 16-bit read only register. It holds the Data portion of the 1st readback word sent back to the V233 by the PSI as a result of the transmitted command.

V233 Function Generator

Ch X Readback ID 2 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 2nd readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored. (Depending on the Frame ID contained in the transmitted command, there may not be a 2nd readback word.)

Ch X Readback Data 2 Register

This is a 16-bit read only register. It holds the Data portion of the 2nd readback word sent back to the V233 as a result of the transmitted command. Depending on the Frame ID contained in the transmitted command, there may not be a 2nd readback word.

Ch X Readback ID 3 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 3rd readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored. (Depending on the Frame ID contained in the transmitted command, there may not be a 3rd readback word.)

Ch X Readback Data 3 Register

This is a 16-bit read only register. It holds the Data portion of the 3rd readback word sent back to the V233 as a result of the transmitted command. Depending on the Frame ID contained in the transmitted command, there may not be a 3rd readback word.

Ch X Readback ID 4 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 4th readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored. (Depending on the Frame ID contained in the transmitted command, there may not be a 4th readback word.)

Ch X Readback Data 4 Register

This is a 16-bit read only register. It holds the Data portion of the 4th readback word sent back to the V233 as a result of the transmitted command. Depending on the Frame ID contained in the transmitted command, there may not be a 4th readback word.

Ch X Readback ID 5 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 5th readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored. (Depending on the Frame ID contained in the transmitted command, there may not be a 5th readback word.)

Ch X Readback Data 5 Register

This is a 16-bit read only register. It holds the Data portion of the 5th readback word sent back to the V233 as a result of the transmitted command. Depending on the Frame ID contained in the transmitted command, there may not be a 5th readback word.

Ch X Readback ID 6 Register

This is a 16-bit read only register. Bits D7 through D0 hold the Frame ID portion of the 6th readback word sent back to the V233 as a result of the transmitted command. D8 is the CRC Error bit, and is set if a CRC error occurred during reception of the readback. Bits D15 through D9 hold Auxiliary bits 6 through 0 returned in the readback word. Auxiliary bit 7 is not stored. (Depending on the Frame ID contained in the transmitted command, there may not be a 6th readback word.)

Ch X Readback Data 6 Register

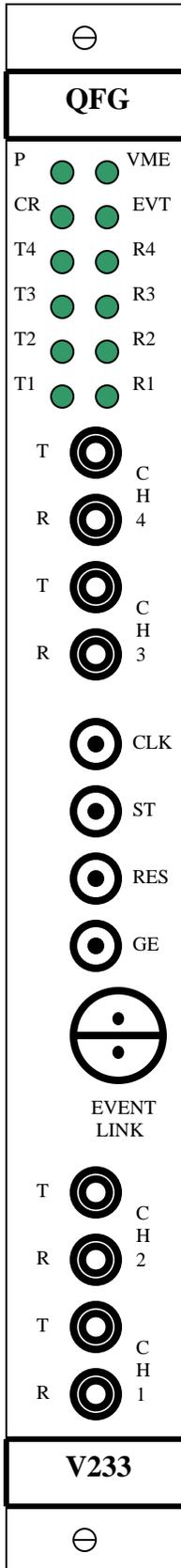
This is a 16-bit read only register. It holds the Data portion of the 6th readback word sent back to the V233 as a result of the transmitted command. Depending on the Frame ID contained in the transmitted command, there may not be a 6th readback word.

As each readback resulting from the transmitted command is decoded and stored in its appropriate register, a counter is incremented and its output is latched into the Ch X Readback Count Register. The counter and the register are both cleared when a command is initially sent to a PSI.

Ch X Readback Count Register

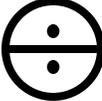
This is an 8-bit read only register that maintains a running count of the number of readbacks received from the PSI as a result of the transmitted command. The count value in this register indicates which readback registers have been updated following a command, because the readbacks are stored sequentially. The minimum value ever seen in this register after a transmitted command is 1, because the minimum number of readbacks words for any command is 1. The maximum value ever seen in this register is 6, because the maximum number of readbacks words for any command is 6.

FRONT PANEL LAYOUT



Representative Drawing of the V233, Revision A, Front Panel.
Not Drawn To Scale.

KEY

-  LED
-  LEMO Connector
-  TWIN-AX Bulkhead Connector
-  T
-  R
-  Front Panel Screw



Front Panel Ejectors



FRONT PANEL LED INDICATORS

There are 12 green front panel LEDs that provide visual status indications of basic module functions.

P (Power)

The top left Power indicator gives visual verification that the onboard power is present. It is tied to the +5V power acquired from the VME backplane. This LED does not give any indication whether the 3 on-board voltage regulators are working properly.

VME

The top right VME indicator lights up whenever a VME data transfer occurs between the V233 module and the VME controller produces an active DTACK* signal. The signal to the LED is pulse stretched in order to be easily observable.

CR (Event Link Carrier)

This indicator is on when the Event Link input is connected and the 10MHz carrier is present.

EVT (Event Link Word)

The EVT indicator lights up whenever a valid Event Link word is decoded. The input to this LED is pulse stretched, which makes it easier to be observed. Under normal working conditions with an active Event Link, this LED will always be on.

T1, T2, T3, T4 (Transmit To PSI)

There is one indicator for each of the 4 fiber optic output channels to the PSI. Whenever a setpoint or a command is sent to a PSI, its corresponding LED is illuminated. The inputs to these LEDs are pulse stretched. During transmission of a function, the Transmit LEDs will always be on.

R1, R2, R3, R4 (Receive From PSI)

There is one indicator for each of the 4 fiber optic input channels from the PSI. When a valid readback word from a PSI is decoded, its corresponding LED is illuminated. The inputs to these LEDs are pulse stretched. During transmission of a function, assuming there is a normal connection to a PSI, the Receive LEDs will always be on.

If no readbacks are received because nothing is being sent to the PSI, this LED will indicate whether the 50MHz carrier from the PSI is present. If the carrier is active, the LED will flash once every 2 seconds.

FRONT PANEL CONNECTORS

CLK (External Clock)

This LEMO connector provides an optically isolated clock input that can be used as the setpoint clock. This input frequency is divided by 100 prior to use. A sweeping Gauss Clock may be used. The clock's maximum input frequency should not exceed 10MHz.

ST (External Start Pulse)

This LEMO connector provides an optically isolated input that can be used like a decoded Event Link word to start a function. The duration of the positive input pulse must be at least 30 nanoseconds. There is no maximum limit to the pulse's length, because it is the positive edge of the pulse that is recognized.

RES (External Resume Pulse)

This LEMO connector provides an optically isolated input so that can be used like a decoded Event Link word to resume a function. It will resume any function that has been paused by setting bit D16 of a setpoint word. The duration of the input pulse must be at least 30 nanoseconds. There is no maximum limit to the pulse's length, because it is the positive edge of the pulse that is recognized.

The V233 can also be configured to use the RES input as a TAG input instead. This function is described later in this document.

GE (External Group End Pulse)

This LEMO connector provides an optically isolated input so that a positive going pulse can be used like a decoded Event Link word to end a function and switch setpoint and readback buffers. The duration of the input pulse must be at least 30 nanoseconds long. There is no maximum limit to the pulse's length, because it is the positive edge of the pulse that is recognized. The 30ns requirement provides a means to de-glitch the input.

EVENT LINK

The Event Link is brought into the V233 module through this BNC twin-ax connector, and is transformer coupled. The V233 will properly decode the Event Link even if the connector is wired with incorrect polarity.

CH1 T/R, CH2 T/R, CH3 T/R, CH4 T/R

These are the 4 sets of fiber optic ST type connectors used for interfacing with PSIs. Each channel's top ST connector is transmitted data, and should be connected to the receive connector of the PSI. The channel's bottom ST connector is for received data, and should be connected to the transmit connector of the PSI.

BACKPLANE CONNECTORS

There are two 160-pin VME backplane connectors on the V233 module. They are designated P1 and P2. The 2 outside pin rows of each connector, designated “z” and “d”, are not used to carry any signals. The remaining 96 pins of each connector are used for the standard VME power, ground, address bus, data bus, and control bus lines. In addition, P2 distributes timing pulse outputs as defined below.

P2

Pin A1:	Channel 1 Timing Pulse	Pin C1:	Ground
Pin A2:	Channel 2 Timing Pulse	Pin C2:	Ground
Pin A3:	Channel 3 Timing Pulse	Pin C3:	Ground
Pin A4:	Channel 4 Timing Pulse	Pin C4:	Ground
Pin A5:	Channel 5 Timing Pulse	Pin C5:	Ground
Pin A6:	Channel 6 Timing Pulse	Pin C6:	Ground
Pin A7:	Channel 7 Timing Pulse	Pin C7:	Ground
Pin A8:	Channel 8 Timing Pulse	Pin C8:	Ground
Pin A9:	Channel 9 Timing Pulse	Pin C9:	Ground
Pin A10:	Channel 10 Timing Pulse	Pin C10:	Ground
Pin A11:	Channel 11 Timing Pulse	Pin C11:	Ground
Pin A12:	Channel 12 Timing Pulse	Pin C12:	Ground
Pin A13:	Channel 13 Timing Pulse	Pin C13:	Ground
Pin A14:	Channel 14 Timing Pulse	Pin C14:	Ground
Pin A15:	Channel 15 Timing Pulse	Pin C15:	Ground
Pin A16:	Channel 16 Timing Pulse	Pin C16:	Ground
Pin A17:	Channel 17 Timing Pulse	Pin C17:	Ground
Pin A18:	Channel 18 Timing Pulse	Pin C18:	Ground
Pin A19:	Channel 19 Timing Pulse	Pin C19:	Ground
Pin A20:	Channel 20 Timing Pulse	Pin C20:	Ground
Pin A21:	Channel 21 Timing Pulse	Pin C21:	Ground
Pin A22:	Channel 22 Timing Pulse	Pin C22:	Ground
Pin A23:	Channel 23 Timing Pulse	Pin C23:	Ground
Pin A24:	Channel 24 Timing Pulse	Pin C24:	Ground
Pin A25:	Channel 25 Timing Pulse	Pin C25:	Ground
Pin A26:	Channel 26 Timing Pulse	Pin C26:	Ground
Pin A27:	Channel 27 Timing Pulse	Pin C27:	Ground
Pin A28:	Channel 28 Timing Pulse	Pin C28:	Ground
Pin A29:	Channel 29 Timing Pulse	Pin C29:	Ground
Pin A30:	Channel 30 Timing Pulse	Pin C30:	Ground
Pin A31:	Channel 31 Timing Pulse	Pin C31:	Ground
Pin A32:	Channel 32 Timing Pulse	Pin C32:	Ground

VME INTERFACE

The V233 module requires both an A24 base address and an A32 base address. All setpoints and readbacks are accessed using A32/D32 VME data transfers. Everything else uses A24/D16 or A24/D08(EO) VME data transfers. To avoid potential conflicts with other V233s or other types of boards that may reside in the same VME chassis, the following base addresses have been reserved for V233s and V133s:

<u>A24</u>	<u>A32</u>
0D0000h	03000000h
0D4000h	03400000h
0D8000h	03800000h
0DC000h	03C00000h
0E0000h	04000000h
0E4000h	04400000h
0E8000h	04800000h
0EC000h	04C00000h

A24 base address 0D0000h should be assigned to the first V233 module in a chassis, followed by 0D4000h, 0D8000h, and so on. The A32 base addresses should be assigned in the same sequence as the A24 base addresses. It would be prudent to keep the same A24 and A32 address pairs as shown above.

The V233 module uses S1, a 10-position SIP switch, to set the board's A24 base address. S2, another 10-position SIP switch located next to S1, is used to set the A32 base address. Each end of the SIP switches are marked with their corresponding address bit positions. S1 covers address bits A14 to A23, and S2 covers address bits A22 to A31.

Each switch is also marked with a "0" on one side and a "1" on the other to indicate which way the contacts must be pushed in order to set or clear an address bit. To set a base address bit high, the contact must be pushed to the "1" side.

During an A24 VME data transfer, when address bits A23-A14 match the settings of S1, and the address modifier code is either 39h or 3Dh, the V233 module will respond. During an A32 VME data transfer, when address bits A31-A22 match the settings of S2, and the address modifier code is either 09h or 0Dh, the V233 module will respond.

Many registers in the V233 use 16 bits. However, there are certain registers that only contain 8 bits of useful content. These registers always use the low data byte, found at odd addresses. See Appendix A and Appendix B for a list of registers and their address assignments.

BOARD IDENTIFICATION

The V233 module may be identified remotely by reading the VME ID message programmed into the V233 module’s main FPGA. The message identifies the module type, revision letter, and serial number of the module. It resides in a read-only register area of the FPGA, from A24 base address + 0000h to + 001Fh. The contents of these registers are ASCII representations, except for those registers holding the value 00h, which is used for spacing purposes.

Starting at the first address, the VME ID should read as follows:

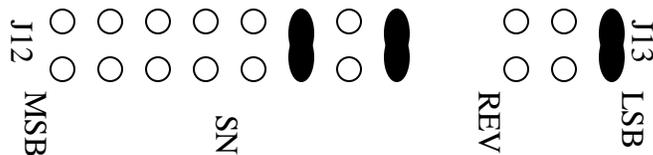
VMEIDBNLV233(00h)(00h)REVx(00h)(00h)SER#xxxx(00h)(00h) (00h)(00h)

The serial number and revision letter of each V233 module are determined by soldering jumpers across the on-board pin sockets of J12 and J13 respectively. J12 is a 2x8 configuration, and J13 is a 2x3 configuration. The sockets should have the appropriate jumpers soldered into them at the time the board is programmed. The jumpers essentially constitute binary counts for both the serial number and the revision letter.

If there are no jumpers in J12, the binary count is 0, and the serial number of the board is 1. If one jumper is soldered into the LSB (Least Significant Bit) position of J12, the binary count is 1, and the serial number of the board is 2, and so on. There are eight jumper positions in J12, allowing for serial numbers 1 through 256.

If there are no jumpers in J13, the revision letter of the board is A. If one jumper is soldered into the LSB position of J13, the serial number of the board is B, and so on. There are three jumper positions in J13, allowing for revision letters A through H.

J12 and J13 are aligned on the V233 so they form a straight line. The letters “LSB” are silk screened at one end of J13, and the letters “MSB” (Most Significant Bit) are silk screened at the other end of J12. The LSB pin sockets for J12 and J13 are the ones closest to the LSB board marking. The MSB pin sockets for J12 and J13 are the ones closest to the MSB board marking.



In the example above, J13 has its LSB jumped. This indicates that the V233 is a revision “B” module. J12 is jumped to a binary count of 5, indicating that this board is serial number 6.

EVENT LINK DECODING

The bi-phase mark encoded Event Link is brought into the V233 module through the front panel twin-ax connector. It is transformer coupled, and then fed to differential receiver U23. The output of the receiver is fed directly to U42, which is the module's main FPGA. As long as the Event Link carrier is present, meaning the Event Link is continuously transitioning, the green CR indicator on the front panel will be on. If the carrier goes down, the CR indicator will turn off. In an idle state, the Event Link delivers a continuous string of "1's"

Inside the main gate array, a 100MHz clock is used to help convert the bi-phase mark encoded data into an NRZL formatted data stream. If the Event Link is inadvertently wired backwards, internal logic still allows the data to be properly converted to an NRZL format. A synchronized in-phase 10MHz clock is derived from the Event Link itself, and accompanies the NRZL data. This derived clock has a small amount of jitter added to it inside the gate array, nominally about 5 nanoseconds. The NRZL data is continually shifted into a shift register and tested for the conditions that determine when a valid Event Link word has been received. Each decoded event is presented in parallel to the 4 channel FPGAs. The synchronized 10MHz clock and various strobes are included for timing purposes.

If the Event Link is running but there are no data words, the 10MHz clock will still be synchronized to the Event Link. In this state, the green EVT indicator on the front panel will be off. Each time a valid Event Link word is decoded, the EVT indicator is turned on. Normally, events appear so rapidly on the Event Link that the EVT indicator is constantly on.

There are 5 conditions that are used to determine when a valid Event Link word has been received. These conditions are as follows.

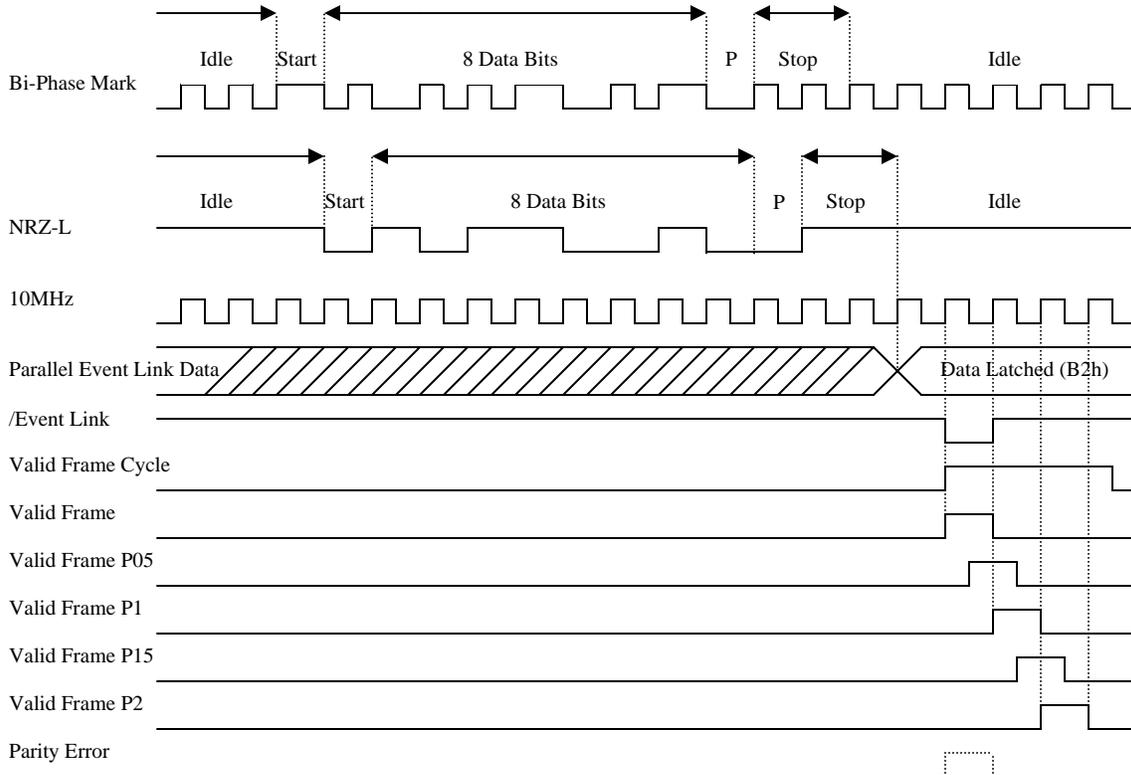
- 1) Word preceded by 2 high bits (idle bits, or the previous word's stop bits)
- 2) 1 start bit (low)
- 3) 8 data bits
- 4) 1 parity bit (even)
- 5) 2 stop bits (high)

If all but the correct parity condition is met, a parity error is declared. If enabled, a parity interrupt will be generated. An Event Link word received with a parity error is considered invalid, and will not be presented to the channel FPGAs.

Once the first Event Link word is decoded correctly and declared valid, a counter is used to allow the minimum number of clocks to expire before checking for the next valid word. This prevents the possibility of decoding certain bit patterns within consecutive words as another valid event.

V233 Function Generator

The figure below shows the timing relationships between the Event Link input and the various decoded Event Link signals generated by the main FPGA.



Notice that the Parity Error strobe is drawn with dashed lines. This is done to show the position of the Parity Error strobe in relation to the Event Link input. If there was a real parity error, none of the other strobes would have been active, and the Event Link data would not be latched into the output buffer.

EVENT LINK SIMULATOR

The V233 provides the means to simulate an Event Link, and generate specific Event Link Words, using the VME interface. The simulated words appear to have been decoded from a live Event Link, and the data is passed to each of the 4 channels. This allows simulation of any type of Event Link word used by the V233...Start Events, Group End Events, User Events, etc. The simulator is intended primarily as a diagnostic tool. Two 8-bit registers are used to control the simulation of an Event Link.

Simulated Event Link Word Register

This is an 8-bit read/write register. Bits D7 through D0 make up the simulated Event Link word.

Event Link Simulator Control Register

This is an 8-bit read/write register that controls the Event Link simulation process. D0 and D1 are the only meaningful bits. D2 -> D7 are not currently used. D0 is automatically cleared after a simulated Event Link word is sent.

- D0 – When set, puts the V233 in Event Link simulator mode. While in simulator mode, no real events are decoded. If an Event Link is still connected, the 10MHz clock used to generate all V233 timing is still derived from the Event Link. If no Event Link is connected, an internal 10MHz clock is used.
- D1 - When set in conjunction with D0 being set, a simulated Event Link word, as defined in the Simulated Event Link Word Register, is presented to each of the 4 channels on the V233.

The location of these registers may be found in Appendix A and Appendix B.

The Simulated Event Link Word Register must be loaded prior to setting bit D1 of the Simulated Event Link Word Register. Setting D1 without D0 being set will not cause a simulated Event Link word to be generated. D1 is automatically cleared.

PPM OPERATION

The V233 module has PPM, or multiple user capability. The V233 may be configured with up to eight individual users. For the purposes of this document, the eight users are identified as user 1 through user 8. PPM capability is a global function. When PPM is used, it is applied to all 4 channels of the board. The V233 cannot be configured to operate one channel in PPM and another channel without PPM.

When the V233 module is first powered up, it defaults to user 1. A board reset will also re-initialize the board to user 1. If PPM capability is not enabled, the V233 board will operate using only the user 1 registers and settings. If PPM capability is disabled after being enabled, the V233 board will revert back to the user 1 settings, regardless of what user it was operating in when the PPM capability was disabled.

All start and resume delays for each channel of the V233 module can be configured on a user-by-user basis. In other words, each user has a unique set of control registers for programming the delays. A user's delay registers are enabled when that user is active. In addition, separate 1 Mbyte sections of DRAM are reserved for storing user setpoints. All other global and channel registers are active across all users.

To configure the V233 module for PPM the following steps must be taken:

- 1) Enable PPM functionality
- 2) Define User Switch Code
- 3) Define User Codes

PPM capability is enabled by setting D8 of the 16-bit User Switch Code register to a value of 1. If D8 of this register is zero, PPM capability is disabled. The User Switch Code register is located at the A24 base address + 40h.

The user switch code is entered into D7->D0 of the User Switch Code register. This defines the Event Link word upon whose occurrence the user will switch.

To enable specific users, D8 of the corresponding 16-bit User Code registers must be set to a value of 1. If D8 of a particular register is zero, that user is disabled. The User 1 Code register is located at the A24 base address + 42h. The User 2 Code register is located at the A24 base address + 44h, and so on, up to the User 8 Code register, which is located at the A24 base address + 50h.

The individual user codes are entered into D7->D0 of the corresponding User Code registers. This defines the Event Link word that determines the next user the V233 module will switch to.

V233 Function Generator

When an Event Link word matches one of the enabled user codes, the V233 prepares to switch to that user. The actual point that the switch takes place is when the user switch code appears on the Event Link. Upon switching users, any active function is halted. When the next Start event occurs, the new user's start delay is loaded into the 24-bit counter, the delay is counted down, and the new user's function commences.

If multiple user codes appear on the Event Link prior to the occurrence of the User Switch Code event, the last user code seen defines which user will become active. If the latest user code to appear is the same as the board's current user, no action will be taken upon the receipt of the user switch code. If no user code appears prior to the receipt of the User Switch code, no action will be taken.

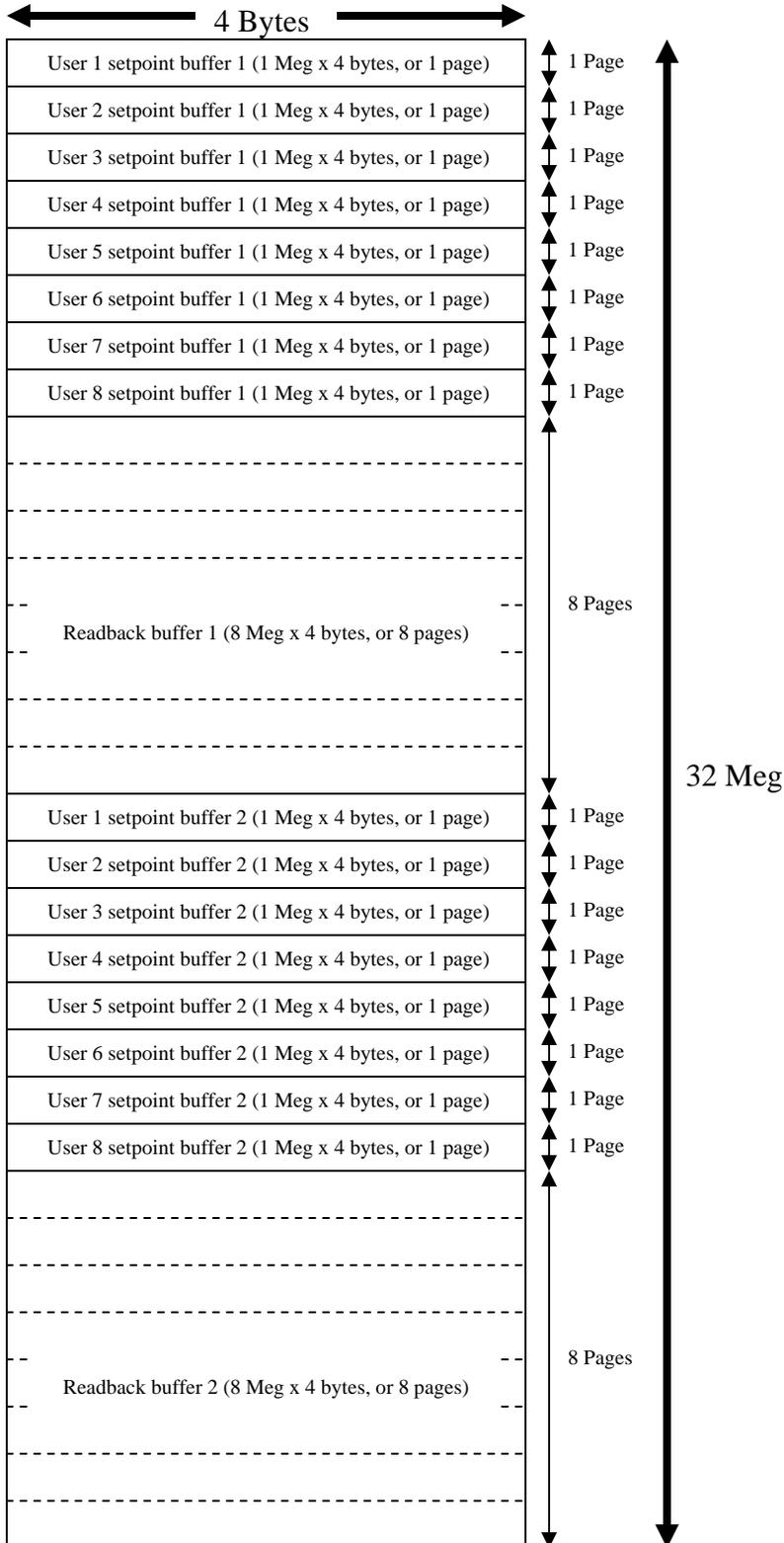
It is significant to note that the Event Link word used as the User Switch Code event may also be defined as a channel's Start event, used by a channel to start a function. This means that users may be switched and a new function started simultaneously.

The 16-bit Main Interrupt Status register and the 16-bit Main Polling Status register, both described in more detail later in this document, each contain three bits that identify the current user. The user is coded into bits D10 -> D8. However, it is possible that the users are being switched very rapidly. Trying to find out if a particular user has been activated may be difficult. To make this easier to do, the V233 module has an 8-bit User History register, located at the A24 base address + 53h. Each bit of this register represents a user. D0 represents user 1, D1 represents user 2, and so on. Whenever a user is activated, its corresponding bit in the User History register is set to a value of 1. If a user is never activated, its bit remains at zero.

The User History register cannot be cleared with a reset. Nor is it cleared automatically when the register is read. Instead, writing a value of 1 to a bit position within the register will clear that bit. Multiple bits can be cleared simultaneously. Writing a value of 0 to a bit position will have no affect.

ADDRESSING SETPOINT AND READBACK BUFFERS

Each channel's DRAM is physically partitioned as shown below.



V233 Function Generator

Setpoint and readback buffers are accessed using A32 addressing and D32 data transfers. D16 and D08(EO) transfers will not work. Since address bits A31-> A22 are used for the module's A32 base address, this leaves 4 Megabytes (1 Meg x 4 bytes) of VME addressing space available to access the DRAM. For the purposes of this document, a 1 Meg x 4 byte section of DRAM is called a "Page". In reality there is much more on-board DRAM space (32 Meg X 4 bytes X 4 channels = 512 Megabytes, or 128 pages) that needs to be addressed. To accomplish this, a "Page" register is used.

Prior to any VME data transfers to or from the DRAM, the Page register must be programmed. The Page register provides the upper address bits needed to access a particular buffer area (page) of DRAM. It can also be used to access either active or inactive buffer areas, without the programmer actually knowing which physical buffer is active and which physical buffer is inactive.

The 16-bit Page register is located at the A24 base address + 20h. Only the lower 9 bits, D8 -> D0, are used. The upper 7 bits are "don't cares". The Page register bit-map is shown below.

Page Register Bit-Map

D8	D7	ADDRESS MODE	D6	D5	DRAM	D4	D3	D2	D1	D0	PAGE (4Mbytes, 1Mword)
0	X	Any Buffer	0	0	Chan 1	0	0	0	0	0	Buffer 1, User 1 Setpoints
1	0	Inactive Buffer (D4 = X)	0	1	Chan 2	0	0	0	0	1	Buffer 1, User 2 Setpoints
1	1	Active Buffer (D4 = X)	1	0	Chan 3	0	0	0	1	0	Buffer 1, User 3 Setpoints
			1	1	Chan 4	0	0	0	1	1	Buffer 1, User 4 Setpoints
						0	0	1	0	0	Buffer 1, User 5 Setpoints
						0	0	1	0	1	Buffer 1, User 6 Setpoints
						0	0	1	1	0	Buffer 1, User 7 Setpoints
						0	0	1	1	1	Buffer 1, User 8 Setpoints
						0	1	0	0	0	Buffer 1, Page 1 Readback
						0	1	0	0	1	Buffer 1, Page 2 Readback
						0	1	0	1	0	Buffer 1, Page 3 Readback
						0	1	0	1	1	Buffer 1, Page 4 Readback
						0	1	1	0	0	Buffer 1, Page 5 Readback
						0	1	1	0	1	Buffer 1, Page 6 Readback
						0	1	1	1	0	Buffer 1, Page 7 Readback
						0	1	1	1	1	Buffer 1, Page 8 Readback
						1	0	0	0	0	Buffer 2, User 1 Setpoints
						1	0	0	0	1	Buffer 2, User 2 Setpoints
						1	0	0	1	0	Buffer 2, User 3 Setpoints
						1	0	0	1	1	Buffer 2, User 4 Setpoints
						1	0	1	0	0	Buffer 2, User 5 Setpoints
						1	0	1	0	1	Buffer 2, User 6 Setpoints
						1	0	1	1	0	Buffer 2, User 7 Setpoints
						1	0	1	1	1	Buffer 2, User 8 Setpoints
						1	1	0	0	0	Buffer 2, Page 1 Readback
						1	1	0	0	1	Buffer 2, Page 2 Readback
						1	1	0	1	0	Buffer 2, Page 3 Readback
						1	1	0	1	1	Buffer 2, Page 4 Readback
						1	1	1	0	0	Buffer 2, Page 5 Readback
						1	1	1	0	1	Buffer 2, Page 6 Readback
						1	1	1	1	0	Buffer 2, Page 7 Readback
						1	1	1	1	1	Buffer 2, Page 8 Readback

When D8 = 1, D7 determines whether the active or inactive buffers are accessed. D4 becomes "don't care"

V233 Function Generator

Notice that there are 2 sets of setpoint buffers, Buffer 1 and Buffer 2, which are divided into 8 individual user buffers. There are also 2 readback buffers, Buffer 1 and Buffer 2, which are user independent. The “1” buffers and the “2” buffers take turns being designated the active and inactive buffers, depending on operational conditions. At power up, the “1” buffers default to the active state, and the “2” buffers are inactive.

When D8 of the Page register is cleared (0), the VME transfer can be for any active or inactive buffer. In this case, D7 of the Page register is a “don’t care” bit. However, when D8 is set (1), D7 determines whether the access is for an active or inactive buffer. If D8 is set and D7 is zero, the access is for an inactive buffer. If D8 is set and D7 is set, the access is for an active buffer.

D6 and D5 of the Page register combine to determine which channel’s buffers are being accessed.

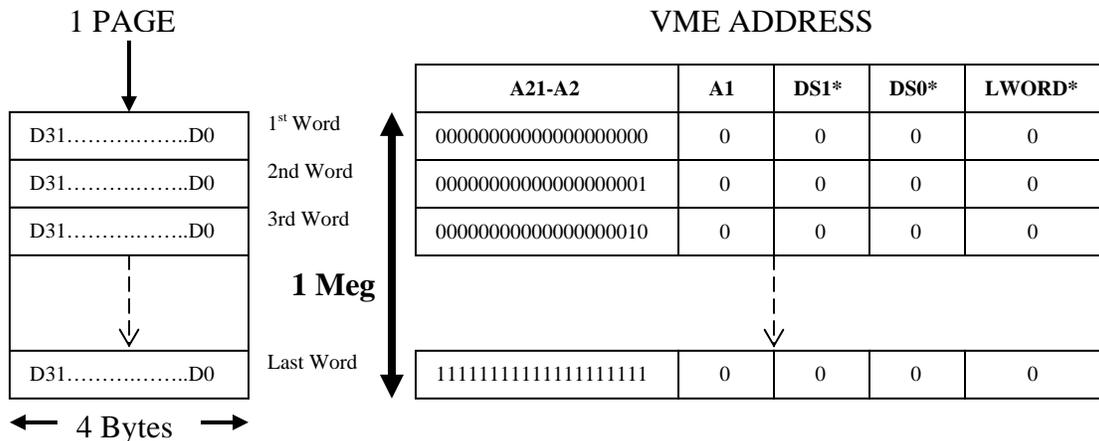
D4 normally determines whether a “1” buffer or a “2” buffer is accessed. However, if D8 is set, D4 essentially becomes a “don’t care” bit, because D7 determines whether the access is for an active or inactive buffer. In this case, D4 is determined internally by the state of the selected channel’s Active Buffer register. (Discussed later in this document)

When D3 is cleared (0), the VME transfer is for one of the user setpoint buffers. When D3 is set (1), the VME transfer is for one of the 8 pages of a readback buffer.

The state of D2 through D0 determines which user setpoint buffer or which page of the readback buffer is addressed.

Once the Page register is set, individual setpoints or readbacks can be written to or read from the selected page with normal A32/D32 VME data transfers.

The VME addressing requirements for a single page using 32-bit transfers is shown below. Remember, the Page register must be properly programmed to access the desired page.



V233 Function Generator

It should be noted that any user setpoint buffer, active or inactive, is exactly 1 page in size. This means the Page register only needs to be programmed once prior to accessing an entire user setpoint buffer. However, a readback buffer spans 8 pages. This means that if all 8 Meg of a readback buffer were to be read, the Page register would have to be programmed 8 times during the read process...Once prior to reading the 1st page, then again prior to reading the 2nd page, and so on, until all 8 pages have been read.

Setpoint buffers may be read at any time without interfering with the Function Generator's operation. However, the programmer should never try to write to an active setpoint buffer while a channel is armed, because the V233 will not actually write the data to the DRAM. If it did, any function being generated might be corrupted, possibly causing damage to a power supply or other devices. If an attempt is made to write to an active setpoint buffer while the channel is armed, the Function Generator will still generate a DTACK* strobe, making it appear to the controller that the write was successful, but the data is ignored.

Readback buffers may also be read at any time without interfering with the Function Generator's operation. In addition, both the active and inactive readback buffers may be written, but doing so while functions are being generated may cause actual readback data to be destroyed. In reality, there is no purpose to write to the readback buffers unless some sort of memory test is being performed, and a memory test should never take place while a channel is armed.

START AND RESUME DELAY MEMORY

As described earlier in the “How A Function Is Sent” section of this document, programmable start delays, as well as programmable resume delays, are generated using a 24-bit down counter. The counter is clocked by a 1MHz clock, providing a programmable delay resolution of 1 microsecond. The delay values are stored in Dual Port RAM, and loaded into the counter when needed. Each channel’s delay memory is resident inside its own FPGA.

Each channel’s user has its own start delay stored in memory. If PPM is not used, the start delay is always stored in the user 1 start delay memory location. If PPM is used, each user must have its start delay memory locations programmed, even if the delays are all the same. When a Start event occurs, the start delay is retrieved from the memory location belonging to the active user, and loaded into the 24-bit down counter. When a VME Start command is issued, the delay counter is cleared, regardless of the programmed start delay values. However, there is always an added delay of 10us built into the start delay process. This delay is fixed, and cannot be changed.

Each channel has 4 separate sets of programmable user resume delays. There are resume 1, resume 2, resume 3, and resume 4 delay memory locations for all 8 users, rendering a total of 32 programmable resume delays per channel. A function is paused by setting any one of 5 bits in a setpoint word. D16 is the pause 1 bit, and enables the resume 1 delay when the function is resumed. D17 is the pause 2 bit, and uses a resume 2 delay. D18 is the pause 3 bit, and uses a resume 3 delay. D19 is the pause 4 bit, and uses a resume 4 delay. D20 is the VME pause bit, and does not use any resume delay. When D20 is set, the function can only be resumed by using a VME Resume command.

If a function does not use any pauses, none of the resume delays need to be programmed. If pauses are used, but the V233 is not being used in PPM mode, only the user 1 resume delay memory location needs to be programmed. Furthermore, only those user 1 resume delay memory locations corresponding to the pause bits actually used in the function need to be programmed. For instance, if PPM is not used, and only D16 is set in any of the function’s setpoints, only the user 1 resume 1 delay memory location needs to be programmed.

When programming the start delay and resume delay memory, the MSB of the delay is D23, and the LSB of the delay is D0. The memory can be accessed using A24/D16 or A24/D08(E0) data transfers, and is formatted in consecutive addresses as shown below.

	High Byte								Low Byte							
Delay Upper Bits	Z	Z	Z	Z	Z	Z	Z	Z	D23	D22	D21	D20	D19	D18	D17	D16
Delay Lower Bits	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

All the start and resume delay memory locations and their address assignments can be found in Appendix A and Appendix B.

CLOCK SELECT REGISTER

Each channel has its own 8-bit Clock Select register. This Read/Write register is used to configure the channel's setpoint clock, and to enable or disable the external inputs. The Clock Select register should be programmed prior to arming the channel. The format of the Clock Select register is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
EXT GE	EXT RES	EXT ST	CLK SEL	GAUSS	CLK 2	CLK 1	CLK 0

D7, when set, enables the external Group End pulse input. If the Group End event is also enabled, the occurrence of an external Group End pulse, a Group End event, or a VME Group End command will be seen as a valid Group End event.

D6, when set, enables the external Resume pulse input. If the Resume 1 event is also enabled, the occurrence of an external Resume pulse or a Resume 1 event will be seen as a valid Resume 1 event.

D5, when set, enables the external Start pulse input. If the Start event is also enabled, the occurrence of an external Start pulse, a Start event, or a VME Start command will be seen as a valid Start event.

D4, when set, uses an on-board 100MHz oscillator to generate various clocks needed to operate the V233. When D3 is cleared, these clocks are derived from the Event Link. D4 needs to be set if there is no Event Link, otherwise the board will not function properly. However, when the Event Link is used and D4 is set, there will be reduced synchronization and repeatability between events on the Event Link and the output to the PSI. If the Event Link is available, it is recommended that D4 be cleared.

D3, when set, forces the V233 to use the external Gauss Clock input as the setpoint clock. This input frequency is divided by 100 before being applied as the setpoint clock. The maximum input clock frequency is 10MHz. All internal clocks will still be derived from the Event Link or the internal oscillator, depending upon the state of D4. Unless the external clock input is synchronized to the Event Link, synchronization and repeatability will be reduced, even with D4 cleared.

When D3 is cleared, the setpoint clock is derived from the Event Link or the internal oscillator, depending on the state of D4. In either case, the state of D2, D1, and D0 combine to determine the setpoint clock frequency. See the table below for the available setpoint clock frequencies.

V233 Function Generator

D3	D2	D1	D0	Setpoint Clock
1	X	X	X	Gauss Clock
0	0	0	0	10KHz
0	0	0	1	1KHz
0	0	1	0	100Hz
0	0	1	1	100KHz
1	1	X	X	1MHz

At power-up, the value of the Clock Select register is 00h. In this state, none of the external inputs are enabled, and all operational clocks are derived from the Event Link. The default setpoint clock is 10KHz.

A setpoint clock of 1MHz does not allow enough time for the PSI to respond to a setpoint with any readbacks. This setting cannot be used for normal operation with a PSI.

The address of each channel's Clock Select register can be found in both Appendix A and Appendix B.

FRAME ID REGISTER

Each channel has its own 8-bit Frame ID register. This Read/Write register defines the Frame ID that will be sent out with each formatted setpoint. This must be programmed prior to arming the channel.

D7 -> D0 define the value of the Frame ID. The normal Frame ID is 15h.

The address of each channel's Frame ID register can be found in Appendix A and Appendix B.

START EVENT REGISTER

Each channel has its own 16-bit Start Event register. This Read/Write register is used to select and enable the channel’s Event Link Start event. The Start Event register should be programmed prior to arming the channel. The format of the Start Event register is shown below.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 are “don’t care” bits.

D8, when set, enables the V233 to search for and use an Event Link Start event.

D7 -> D0 define the value of the Start event.

When D8 is zero, the V233 will not decode an Event Link Start event, regardless of the contents of D7 -> D0.

The address of each channel’s Start Event register can be found in Appendix A and Appendix B.

RESUME EVENT REGISTERS

Each channel has four 16-bit Resume Event registers. These Read/Write register are used to select and enable each of the channel’s Resume events. The Resume Event registers should be programmed prior to arming the channel. The format of the Resume Event registers is shown below.

Resume Event 1 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Resume Event 2 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Resume Event 3 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Resume Event 4 Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 are “don’t care” bits.

D8, when set, enables the V233 to search for and use the Event Link Resume event.

D7 -> D0 define the value of the Resume event.

When D8 is zero, the V233 will not decode the Event Link Resume event, regardless of the contents of D7 -> D0.

The addresses of each channel’s Resume Event registers can be found in Appendix A and Appendix B.

GROUP END EVENT REGISTER

Each channel has its own 16-bit Group End Event register. This Read/Write register is used to select and enable the channel’s Event Link Group End event. The Group End Event register should be programmed prior to arming the channel. The format of the Group End Event register is shown below.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	U2	U1	U0	HLTD	HLT	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D14 are “don’t care” bits.

D13 -> D11 represents the user during which the last function will be sent prior to the channel being “halted”. 000 = user 1, 001 = user 2, etc.

D10, when set, indicates that the channel was halted after sending the last function. This bit must be cleared before a new function will be allowed to start.

D9, when set, tells the channel to halt after the first function in the selected user is sent. The halt utility does not “arm” until the next Group End event following D9 being set. Any functions programmed for users appearing before the selected user will be sent in the normal manner. After the first function in the selected user is sent, the last setpoint of that function is repeated until another Group End event occurs, regardless of subsequent Start events or any user changes. Once that Group End event occurs, all setpoints will stop. No new functions can be sent until D10 is cleared and another Group End event occurs, resetting the channel.

D8, when set, enables the V233 to search for and use an Event Link Group End event.

D7 -> D0 define the value of the Group End event.

When D8 is zero, the V233 will not decode an Event Link Group End event, regardless of the contents of D7 -> D0.

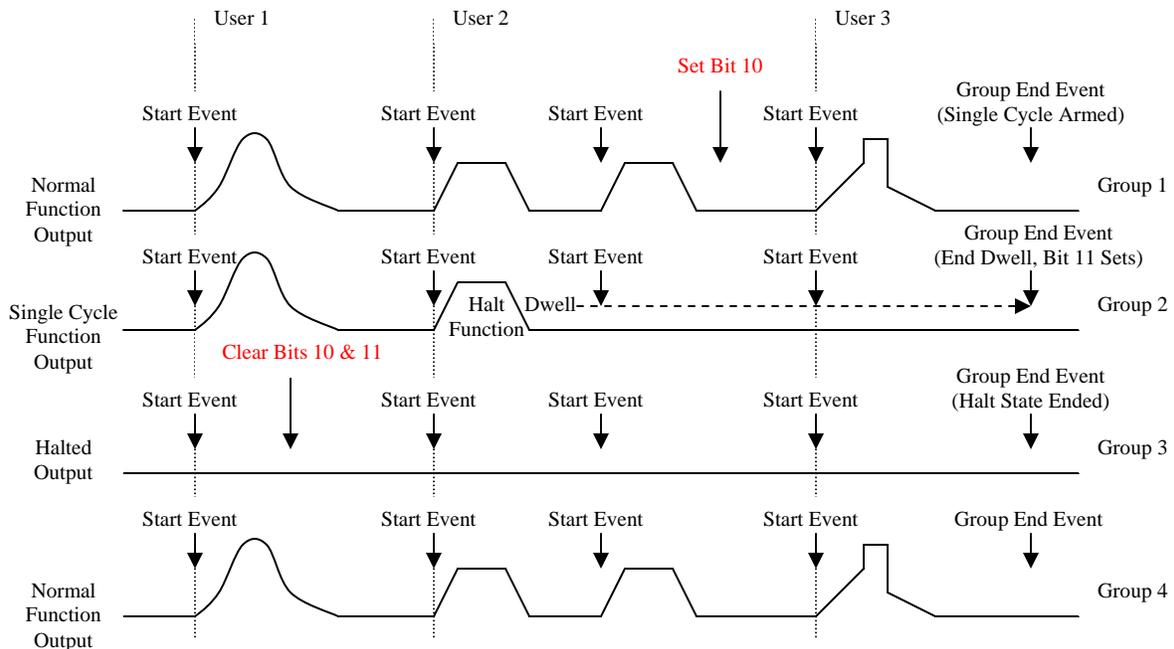
The address of each channel’s Group End Event register can be found in Appendix A and Appendix B.

SINGLE CYCLE OPERATION

For power supply testing purposes it is sometimes desirable to operate a V233 channel in Single Cycle mode. In Single Cycle mode, a channel is programmed to stop generating any new functions after the first function in a designated user has been sent. This function will be known as the halt function. The Single Cycle mode works as follows:

- 1) Set the Halt bit (D9) of the channel's Group End register. Also load the desired user in bits D13 - D11. 000 = user 1, 001 = user 2, etc.
- 2) Upon the next Group End event, the single cycle utility is armed. The Single Cycle mode can still be cancelled by clearing bit 10 of the Group End register anytime before the halt function starts.
- 3) The first Start event occurring during the designated user will cause the halt function to begin. The Single Cycle mode cannot be cancelled at this point.
- 4) When the last setpoint of the halt function is reached, it is repeated until the next Group End event occurs. This is known as dwelling. The dwell will continue regardless of any subsequent Start events or User Switch events. During dwell, the V233 will continue to receive and store readbacks. A change in user will be noted by a corresponding change in the overhead bits of the readback words.
- 5) At Group End, all setpoints cease, the channel is halted, and Bit 11 of the Group End register is set. No further functions will be generated.
- 6) Clearing bit 11 of the Group End register, followed by the occurrence of another Group End event, will end the halt state. If bit 10 remains set, another single cycle will be armed. If bit 10 is cleared along with bit 11, the channel will return to normal operation.

The timing diagram below illustrates how a channel's normal behavior would change if configured to perform a single cycle during user 2.



TAG EVENT REGISTER

A tag is used to identify a group of readbacks with a specific event or external input pulse. When the Tag event or external tag input pulse occurs, the next setpoint sent out will cause its readbacks to have bit D25 set. D25 is the EOT/Tag bit in the formatted readback word. The subsequent setpoint will clear the tag.

Each channel has its own 16-bit Tag Event register. This Read/Write register is used to select and enable the channel’s Event Link Tag event. The format of the Tag Event register is shown below.

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	EXT	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 are “don’t care” bits.

D9, when set, indicates that the external Tag input is enabled. The external Resume input doubles as the external Tag input. If used as a Tag input, the Resume input is disabled, but only for the channel that has D9 set in its Tag Event register.

D8, when set, enables the V233 to search for and use an Event Link Tag event.

D7 -> D0 define the value of the Tag event.

When D8 is zero, the V233 will not decode a Tag event, regardless of the contents of D7 -> D0.

The address of each channel’s Tag Event register can be found in Appendix A and Appendix B.

ARMING CHANNELS

Each of the 4 channels is armed using the global Channel Arm register. This is an 8-bit Read/Write register, located at the A24 base address + 2Fh. The Channel Arm register should be the last register programmed in preparation of generating a function. The format of the Channel Arm register is shown below.

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	CH4	CH3	CH2	CH1

D7 -> D4 are “don’t care” bits.

D3, when set, arms channel 4. Clearing D3 dis-arms channel 4.

D2, when set, arms channel 3. Clearing D3 dis-arms channel 3.

D1, when set, arms channel 2. Clearing D3 dis-arms channel 2.

D0, when set, arms channel 1. Clearing D3 dis-arms channel 1.

Dis-arming a channel immediately halts setpoint transmission and readback storage. It also resets the readback buffer address generator, as well as the channel’s setpoint counter. Dis-arming a channel does not change any values in the various control and configuration registers, nor does it prevent Group End from switching the active and inactive readback buffers.

SETPOINT COUNT REGISTERS

Each channel has an 8-bit Setpoint Count High register and a 16-bit Setpoint Count Low register. These Read Only registers are used to store the number of setpoints sent to a PSI between Group End events. The format of the registers is shown below.

Setpoint Count High Register

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Setpoint Count Low Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Each channel has a 24-bit counter that keeps track of the number of setpoints sent to the PSI. The counter’s output is latched into the Setpoint Count registers upon the occurrence of Group End, and then cleared.

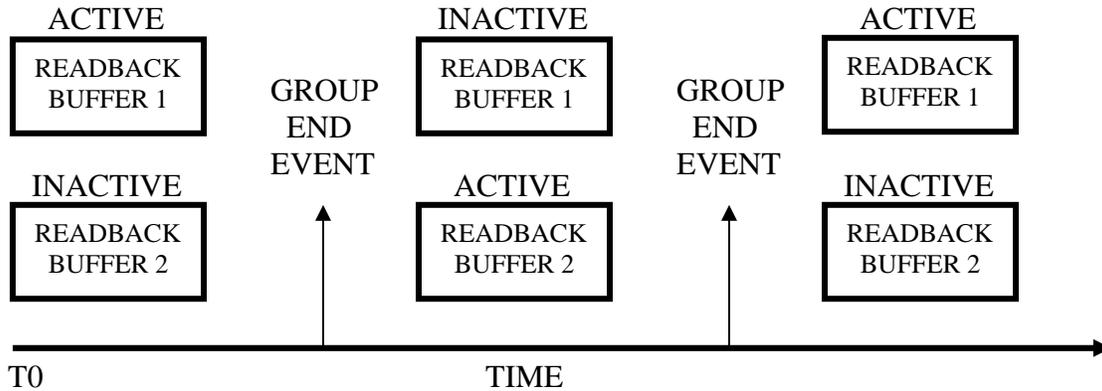
The maximum value the counter will hold is 16,777,215. The LSB of the count is stored in bit D0 of the Setpoint Count Low register. The MSB of the count is stored in bit D7 of the Setpoint Count High register.

The addresses of each channel’s Setpoint Count High register and Setpoint Count Low register can be found in Appendix A and Appendix B.

SWITCHING READBACK AND SETPOINT BUFFERS

Readback Buffers

Each channel’s active and inactive readback buffers are automatically upon every Group End event, external Group End pulse, or VME Group End command. The switch occurs whether a channel is armed or dis-armed.



Setpoint Buffers

Setpoint buffers are different from readback buffers in 2 primary ways. First, there are separate setpoint buffer areas for 8 users. Second, each user setpoint buffer will only switch on the Group End event if instructed to do so.

Each user of each channel has control over when its setpoint buffers get switched. This is done through the User X Switch Active Buffer registers. The Switch Active Buffer registers are 8-bit Write Only registers. If D0 is set when Group End occurs, that user’s setpoint buffers are switched. D0 is automatically cleared upon the occurrence of Group End. The register is formatted as shown below.

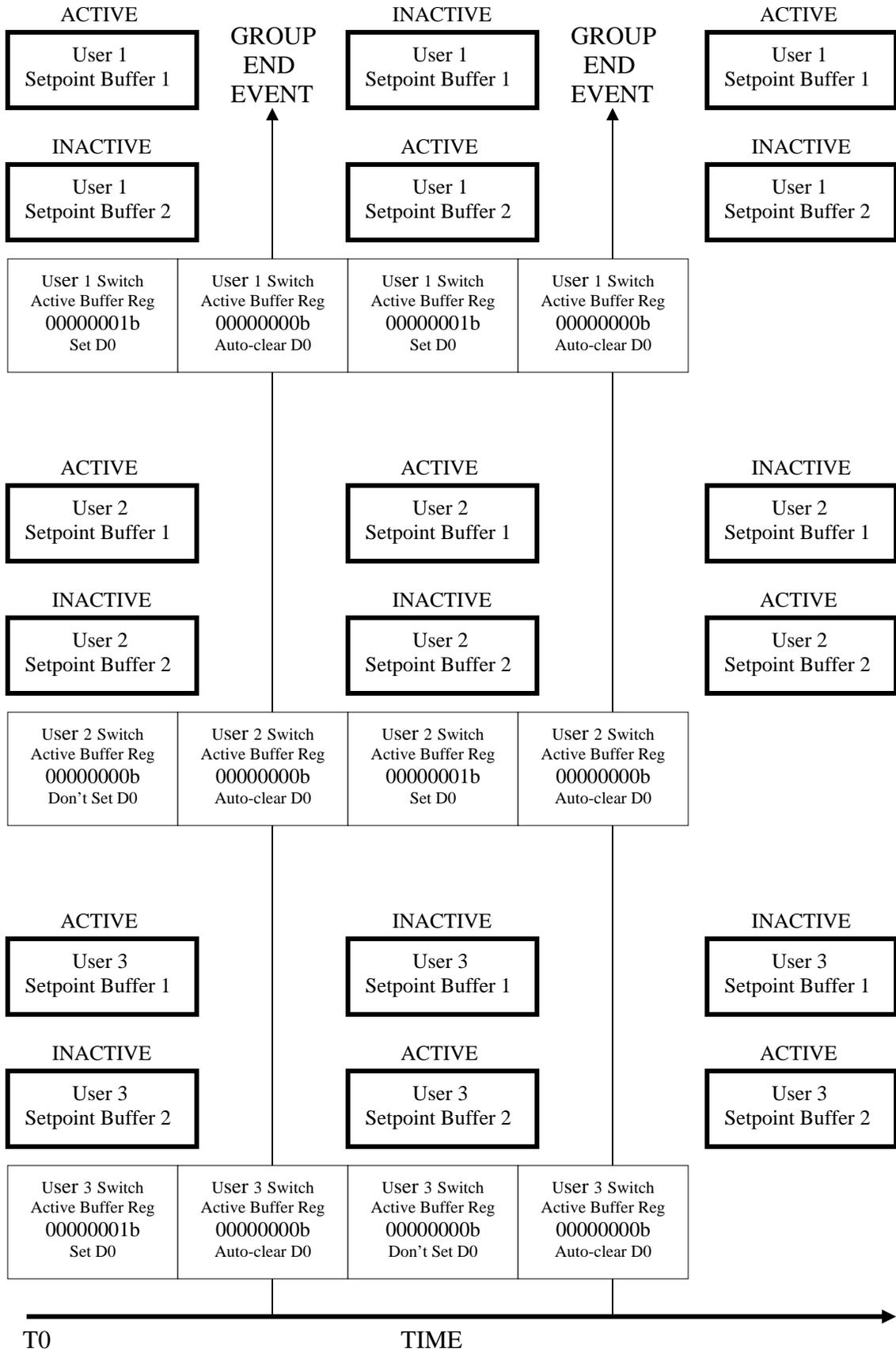
User X Switch Active Buffer Register

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	Z	Z	Z	1/0

D0, when set, tells the user setpoint buffers to switch upon Group End.

The examples on the next page show user setpoint buffers being switched using the User Switch Active Buffer registers and the Group End event.

V233 Function Generator



V233 Function Generator

At T0, user 1, user 2, and user 3 all have buffer 1 set as their active buffer. The User 1 and User 2 Switch Active Buffer registers have D0 set, indicating that user 1 and user 3 will switch buffers when Group End occurs.

At the first Group End, the user 1 and user 3 buffers switch, and their Switch Active Buffer registers are cleared. The user 2 buffers do not switch.

Then the User 1 and User 2 Switch Active Buffer registers have D0 set, indicating that user 1 and user 2 will switch buffers when the next Group End occurs.

At the second Group End, the user 1 and user 2 buffers switch, and their Switch Active Buffer registers are cleared. The user 3 buffers do not switch.

If there are many V233s in a system, problems may be encountered getting all the boards to switch their selected setpoint buffers at the same time. For instance, a Group End event may occur before all the Switch Active Buffer registers have been set up. To synchronize the buffer switching process across boards, use the global Switch Buffer Ready register. This 16-bit Read/Write register is used to select and enable the board's Event Link Switch Buffer Ready event. The format of the register is shown below.

Switch Buffer Ready Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	E	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 are “don't care” bits.

D8, when set, forces the V233 to wait for a Switch Buffer Ready event before a Group End Event can switch the selected setpoint buffers. If D8 is set, and a Switch Buffer Ready event doesn't occur, the setpoint buffers will not switch upon a Group End event. Once a Switch Buffer Ready event occurs, the switching mechanism is “armed”, and the next Group End event will cause the selected setpoint buffers to switch. The switching mechanism is the “dis-armed”, and a subsequent Switch Buffer Ready event must occur before another switch can occur. If D8 is cleared, selected setpoint buffers will switch when the first Group End Event occurs.

D7 -> D0 define the value of the Switch Buffer Ready event.

V233 Function Generator

Each channel has an Active Buffers register. This 16-bit Read Only register indicates which readback buffer and which user setpoint buffer is active. It is formatted as shown below.

Active Buffers Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	R	U8	U7	U6	U5	U4	U3	U2	U1

D15 -> D9 are “don’t care” bits.

D8, when set, indicates readback buffer 2 is active. When D8 is cleared, it indicates that readback buffer 1 is active.

D7, when set, indicates user 8 setpoint buffer 2 is active. When D7 is cleared, it indicates that user 8 setpoint buffer 1 is active.

D6, when set, indicates user 7 setpoint buffer 2 is active. When D6 is cleared, it indicates that user 7 setpoint buffer 1 is active.

D5, when set, indicates user 6 setpoint buffer 2 is active. When D5 is cleared, it indicates that user 6 setpoint buffer 1 is active.

D4, when set, indicates user 5 setpoint buffer 2 is active. When D4 is cleared, it indicates that user 5 setpoint buffer 1 is active.

D3, when set, indicates user 4 setpoint buffer 2 is active. When D3 is cleared, it indicates that user 4 setpoint buffer 1 is active.

D2, when set, indicates user 3 setpoint buffer 2 is active. When D2 is cleared, it indicates that user 3 setpoint buffer 1 is active.

D1, when set, indicates user 2 setpoint buffer 2 is active. When D1 is cleared, it indicates that user 2 setpoint buffer 1 is active.

D0, when set, indicates user 1 setpoint buffer 2 is active. When D0 is cleared, it indicates that user 1 setpoint buffer 1 is active.

The address of the Switch Buffer Ready Register, as well as the addresses of each channel’s Switch Active Buffer registers and Active Buffers register, can be found in Appendix A and Appendix B.

SENDING VME COMMANDS

Each channel has its own VME Commands register. This register allows the programmer to send any 1 of 4 possible VME commands.

1. VME Start Command
2. VME Resume Command
3. VME Group End Command
4. VME Tag Command

The VME Commands register is an 8-bit Write Only register, which is automatically cleared as soon as the command is sent. The format is shown below.

VME Commands Register

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	T	GE	R	S

D7 -> D4 cannot be accessed.

D3, when set, initiates a VME Tag command

D2, when set, initiates a VME Group End command.

D1, when set, initiates a VME Resume command.

D0, when set, initiates a VME Start command.

If multiple bits are set, only 1 will be acted upon. The order of priority is D0, D1, D2, and then D3. Once the command is issued, all bits will be cleared.

A VME Start command will not be recognized unless the channel is armed prior to issuing the command. A VME Start command will always have a programmable start delay of zero. However, the built-in 100us delay will be used.

A VME Resume command will only have an affect if a function is in a VME pause. A VME Resume command will always have a programmable resume delay of zero. However, the built-in 100us delay will be used.

A VME Group End command will always be recognized.

A VME Tag command will always be recognized.

INTERRUPTS AND STATUS

The V233 module is capable of generating 3 board level interrupts. In addition, each channel can provide another 14 interrupts. Interrupt selection is independent of PPM mode. Any enabled interrupt is enabled across all users.

Any enabled interrupt condition that occurs, no matter how brief, will cause an interrupt. All interrupt conditions have corresponding bits in 2 identical status register. These bits are latched, so even a transitional condition will be captured.

The interrupt level of the V233 module is programmable, set within the 8-bit Read/Write Interrupt Level register. This register is located at the A24 base address + 23h. A value of 00h written into this register will disable all interrupts. A value of 01h will set the V233 to an interrupt level of 1. A value of 02h will set the V233 to an interrupt level of 2, and so on. The highest interrupt level is 7. The upper 5 bits of this register are ignored. The format of the Interrupt Level register is shown below.

Interrupt Level Register

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	1/0	1/0	1/0

The 16-bit Read/Write Interrupt Vector register, located at the A24 base address + 24h, holds the module's Status/ID word, which is put on the VME bus by the V233 module when its interrupt is serviced. The Status/ID is should be programmed during the board's initial configuration. If the V233 needs to respond to an interrupt with a 16-bit Status/ID word, the contents of the entire register will be put on the bus. If an 8-bit word is required, the lower 8 bits of the register will be put on the bus. The format of the Interrupt Vector register is shown below.

Interrupt Vector Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Each of the 3 board level interrupts can be individually enabled or disabled using the 8-bit Interrupt Enable register, located at A24 base address + 27h. This Read/Write register is also used to enable or disable a pre-selected set of interrupts from each of the 4 channels. The channel interrupts are pre-selected in individual channel Interrupt Enable registers, covered later in this section.

A "1" bit in the Interrupt Enable register enables the corresponding interrupt. A "0" bit disables the corresponding interrupt. If the Interrupt Enable register contains all zeros, all interrupts are disabled. The enabling bits in this register are in the same position as the corresponding status bits in the Main Interrupt Status register and the Main Interrupt Polling register. Reading the Main Interrupt Status register during an interrupt routine will identify the cause of the interrupt.

V233 Function Generator

The following board level interrupts can be enabled in any combination:

1. Event Link Carrier Down.
The V233 module will not issue a Carrier Down interrupt unless an Event Link Carrier Up condition first existed.
2. Event Link Carrier Up.
The V233 module will not issue a Carrier Up interrupt unless a Carrier Down interrupt occurs first, and then the carrier is restored.
3. Event Link Parity Error.

In addition to the board level interrupts, all channel interrupts are globally enabled or disabled in the Interrupt Enable register. The format of the register is shown below.

Interrupt Enable Register

D7	D6	D5	D4	D3	D2	D1	D0
CH4	CH3	CH2	CH1	X	PE	CU	CD

D7, when set, enables the channel 4 interrupts selected in the Ch4 Interrupt Enable register. When D7 is cleared, all channel 4 interrupts are disabled.

D6, when set, enables the channel 3 interrupts selected in the Ch3 Interrupt Enable register. When D6 is cleared, all channel 3 interrupts are disabled.

D5, when set, enables the channel 2 interrupts selected in the Ch2 Interrupt Enable register. When D5 is cleared, all channel 2 interrupts are disabled.

D4, when set, enables the channel 1 interrupts selected in the Ch1 Interrupt Enable register. When D4 is cleared, all channel 1 interrupts are disabled.

D3 is a “don’t care” bit.

D2, when set, enables the Event Link Parity Error interrupt. Any time an Event Link word is decoded with a parity error, this interrupt will be set. When D2 is cleared, the Event Link Parity Error interrupt is disabled.

D1, when set, enables the Event Link Carrier Up interrupt. Any time the Event Link carrier comes back after being down, this interrupt will be set. When D1 is cleared, the Event Link Carrier Up interrupt is disabled.

D0, when set, enables the Event Link Carrier Down interrupt. Any time the Event Link carrier goes down after being up, this interrupt will be set. When D0 is cleared, the Event Link Carrier Down interrupt is disabled.

V233 Function Generator

When handling an interrupt, the Main Interrupt Status register, located at the A24 base address + 28h, can be used to help determine the cause of the interrupt. This is a 16-bit, Read Only register, which is automatically cleared when read. The register's format is shown below.

Main Interrupt Status Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	BR	U	U	U	CH4	CH3	CH2	CH1	EV	PE	CU	CD

D15 -> D12 are not used. They are always zero.

D11, when set, indicates the V233 board is ready for normal operation. When power is cycled or the board is reset, the on-board DRAM goes through an initialization process that takes 160 microseconds. D11 goes high after the initialization process is finished. This bit is not latched, nor is it associated with an interrupt.

D10 -> D8 combine to indicate the active user. These bits are not latched, nor are they associated with an interrupt. The user codes are shown below.

D10	D9	D8	User
0	0	0	User 1
0	0	1	User 2
0	1	0	User 3
0	1	1	User 4
1	0	0	User 5
1	0	1	User 6
1	1	0	User 7
1	1	1	User 8

D7, when set, indicates there was an interrupt from channel 4. This bit is latched. Read the Ch4 Interrupt Status register to determine the cause of the interrupt.

D6, when set, indicates there was an interrupt from channel 3. This bit is latched. Read the Ch3 Interrupt Status register to determine the cause of the interrupt.

D5, when set, indicates there was an interrupt from channel 2. This bit is latched. Read the Ch2 Interrupt Status register to determine the cause of the interrupt.

D4, when set, indicates there was an interrupt from channel 1. This bit is latched. Read the Ch1 Interrupt Status register to determine the cause of the interrupt.

D3, when set, indicates a valid Event Link word was decoded. This bit is latched. There is no associated interrupt with this status bit.

D2, when set, indicates an Event Link word was received with a parity error. This bit is latched.

V233 Function Generator

D1, when set, indicates the Event Link carrier is present. If the status is read while the carrier is still present, the status bit will be cleared, and then immediately set again. After the carrier goes down, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D0, when set, indicates the Event Link carrier is down. If the status is read while the carrier is still down, the status bit will be cleared, and then immediately set again. After the carrier goes up, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

An Event Link Up or Event Link Down interrupt will only be declared upon a state change of the Event Link carrier. If the Event Link is up, and then the carrier is lost, an Event Link Down interrupt will occur. (Assuming the interrupt is enabled) Once the interrupt is handled, clearing the interrupt, no further Event Link Down interrupts will be issued until the Event Link carrier returns, and goes back down again. However, the Event Link Down status bit, D0, will remain set for the duration that the Event Link is actually down. If the Event Link is still down when the status word is read, bit D0 is cleared, then immediately set again. If the Event Link returns, D1 is set, but D0 also remains set until the status word is read. Reading clears all the status bits, including D0 and D1. D0 remains in a zero state, because the Event Link is no longer down. However, D1 is immediately set again, because the Event Link is still up.

Because a status register is automatically cleared every time it is read, the V233 has 2 separate but identical status registers. The Main Polling Status register, located at the A24 base address + 2Ah, is identical to the Main Interrupt Status register. The Main Polling Status register should only be used for any routine polling of the Function Generator's status. Likewise, the Main Interrupt Status register should only be used for acquiring status during an interrupt routine. If there were only 1 channel status register, polling it just after an interrupt occurred, but before it could be read by the interrupt routine, could prematurely clear the status bit. This could mask the true cause of the interrupt.

A system or board level reset will clear the Interrupt Level register, The Interrupt Vector register, and the Interrupt Enable register. It will also clear the lower 8 bits of the Main Interrupt Status register and the Main Polling Status register.

Channel Interrupt Control

As stated earlier, channel interrupts are enabled or disabled globally within the Interrupt Enable register. However, each channel's active interrupts are determined in the Ch 1 Interrupt Enable register, the Ch 2 Interrupt Enable register, the Ch 3 Interrupt Enable register, and the Ch 4 Interrupt Enable register. The address locations of these registers can be found in Appendix A and Appendix B.

Each channel's Interrupt Enable register allows the channel's to have different sets of interruptible conditions. The format of the registers is shown below.

Ch X Interrupt Enable Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RUN	EOF	GE	EE	P4	P3	P2	P1	VP	RB	SP	MR	X	CRC	LU	LD

D15, when set, enables the channel's Run interrupt. When a function is first started, this interrupt is set. A function is considered started when the channel is armed and the first Start event occurs, not necessarily when the first setpoint is sent. Another Run interrupt cannot be issued until a Group End, user change, or reset occurs, followed by another Start event. If the channel is disarmed and then re-armed, the next Start event will also cause a new Run Interrupt to be issued. When D15 is cleared, the channel's Run interrupt is disabled.

D14, when set, enables the channel's End Of Function interrupt. A function is considered ended when the last setpoint in the setpoint buffer is transmitted. This last setpoint is the only one that has overhead bit D31 set high. Even though the last setpoint is repeated until Group End or a user change occurs, the end of the function is defined as the first time the last setpoint is sent. When D14 is cleared, the channel's End Of Function interrupt is disabled.

D13, when set, enables the channel's Group End interrupt. This interrupt will occur whether the channel is armed or not. When D13 is cleared, the channel's Group End interrupt is disabled.

D12, when set, enables the channel's End Of Function Error interrupt. A function is considered to have ended in error if a Group End or user change occurred before the last setpoint of a function was sent. This would prematurely end the function, but an End Of Function interrupt would not be issued under this circumstance. When D12 is cleared, the channel's End Of Function Error interrupt is disabled.

D11, when set, enables the channel's Pause 4 interrupt. This occurs when a function is paused by a sending a setpoint that has overhead bit D19 set high. When D11 is cleared, the channel's Pause 4 interrupt is disabled.

D10, when set, enables the channel's Pause 3 interrupt. This occurs when a function is paused by a sending a setpoint that has overhead bit D18 set high. When D10 is cleared, the channel's Pause 3 interrupt is disabled.

V233 Function Generator

D9, when set, enables the channel's Pause 2 interrupt. This occurs when a function is paused by a sending a setpoint that has overhead bit D17 set high. When D9 is cleared, the channel's Pause 2 interrupt is disabled.

D8, when set, enables the channel's Pause 1 interrupt. This occurs when a function is paused by a sending a setpoint that has overhead bit D16 set high. When D8 is cleared, the channel's Pause 1 interrupt is disabled.

D7, when set, enables the channel's VME Pause interrupt. This occurs when a function is paused by a sending a setpoint that has overhead bit D20 set high. When D7 is cleared, the channel's VME Pause interrupt is disabled.

D6, when set, enables the channel's Readback Overflow interrupt. This occurs when the active readback buffer is full, meaning there has been more than 8 meg of readbacks between Group End events. All subsequent readbacks will be lost, until the readback buffers are switched. When D6 is cleared, the channel's Readback Overflow interrupt is disabled.

D5, when set, enables the channel's Setpoint Overflow interrupt. This occurs when all the setpoints in the active user setpoint buffer have been sent, and none of them had the overhead bit D31 set, indicating it as the last setpoint of the function. This would only occur due to a programming error. Setpoint transmission halts as soon as a setpoint overflow is seen. When D5 is cleared, the channel's Setpoint Overflow interrupt is disabled.

D4, when set, enables the channel's Missing Readback interrupt. This occurs when no readbacks are returned by the PSI between any two consecutive setpoints. When D4 is cleared, the Missing Readback interrupt is disabled.

D3 is a "don't care" bit.

D2, when set, enables the channel's CRC interrupt. Any time a readback word from the PSI is decoded with a CRC error, this interrupt will be set. When D2 is cleared, the CRC interrupt is disabled.

D1, when set, enables the channel's Link Up interrupt. Any time the carrier from the PSI comes back after being down, this interrupt will be set. When D1 is cleared, the Link Up interrupt is disabled.

D0, when set, enables the channel's Link Down interrupt. Any time the carrier from the PSI goes down after being up, this interrupt will be set. When D0 is cleared, the Link Down interrupt is disabled.

V233 Function Generator

When handling interrupts from channels, the Ch 1 Interrupt Status register, Ch 2 Interrupt Status register, Ch 3 Interrupt Status register, and Ch 4 Interrupt Status register can be used to help determine the cause of the interrupt. These are 16-bit, Read Only registers, which are automatically cleared when read. The address locations of these registers can be found in Appendix A and Appendix B. Their format is shown below.

Ch X Interrupt Status Register

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
RUN	EOF	GE	EE	P4	P3	P2	P1	VP	RB	SP	MR	LI	CRC	LU	LD

D15, when set, indicates a function is running. A function runs from the initial Start event until the last setpoint is sent. If the status is read while the function is running, the bit will be cleared, and then immediately set again. After the function has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D14, when set, indicates the last setpoint of a function is being repeated. If the status is read while the last setpoint is still being repeated the bit will be cleared, and then immediately set again. After setpoint transmission has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D13, when set, indicates a Group End event occurred. This input is latched.

D12, when set, indicates an End Of Function Error occurred. This input is latched.

D11, when set, indicates the function is in a pause, initiated by overhead bit D19 of a transmitted setpoint. If the status is read while the function is paused, the status bit will be cleared, and then immediately set again. After the pause has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D10, when set, indicates the function is in a pause, initiated by overhead bit D18 of a transmitted setpoint. If the status is read while the function is paused, the status bit will be cleared, and then immediately set again. After the pause has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D9, when set, indicates the function is in a pause, initiated by overhead bit D17 of a transmitted setpoint. If the status is read while the function is paused, the status bit will be cleared, and then immediately set again. After the pause has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D8, when set, indicates the function is in a pause, initiated by overhead bit D16 of a transmitted setpoint. If the status is read while the function is paused, the status bit will be cleared, and then immediately set again. After the pause has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

V233 Function Generator

D7, when set, indicates the function is in a pause, initiated by a VME Pause command. If the status is read while the function is still paused, the status bit will be cleared, and then immediately set again. After the pause has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D6, when set, indicates the active readback buffer is in an overflow condition. If the status is read while the overflow condition is still active, the status bit will be cleared, and then immediately set again. After the overflow condition has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D5, when set, indicates the active setpoint buffer is in an overflow condition. If the status is read while the overflow condition is still active, the status bit will be cleared, and then immediately set again. After the overflow condition has ended, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D4, when set, indicates no readbacks were received between any two consecutive setpoints. This bit is latched.

D3, when set, indicates a readback word has been received. This bit is latched.

D2, when set, indicates a readback word has been received with a CRC error. This bit is latched.

D1, when set, indicates when the PSI Link input carrier was present. If the status is read while the carrier is still present, the status bit will be cleared, and then immediately set again. After the carrier goes down, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

D0, when set, indicates when the PSI Link input carrier was down. If the status is read while the carrier is still down, the status bit will be cleared, and then immediately set again. After the carrier goes up, the bit will stay set until the status is read. Upon being read, the bit will be cleared and remain at zero.

A PSI Link Up or PSI Link Down interrupt will only be declared upon a state change of the PSI input carrier. If the PSI Link is up, and then the carrier is lost, a PSI Link Down interrupt will occur. (Assuming the interrupt is enabled) Once the interrupt is handled, clearing the interrupt, no further PSI Link Down interrupts will be issued until the PSI input carrier returns, and goes back down again. However, the PSI Link Down status bit, D0, will remain set for the duration that the PSI Link is actually down. If the PSI Link is still down when the status word is read, bit D0 is cleared, then immediately set again. If the PSI Link returns, D1 is set, but D0 also remains set until the status word is read. Reading clears all the status bits, including D0 and D1. D0 remains in a zero state, because the PSI Link is no longer down. However, D1 is immediately set again, because the PSI Link is still up.

V233 Function Generator

Because a channel's status register is automatically cleared every time it is read, the V233 has 2 separate but identical status registers for each channel. The Ch 1 Polling Status register is identical to the Ch 1 Interrupt Status register. The Ch 2 Polling Status register is identical to the Ch 2 Interrupt Status register. The Ch 3 Polling Status register is identical to the Ch 3 Interrupt Status register. The Ch 4 Polling Status register is identical to the Ch 4 Interrupt Status register.

The Ch X Polling Status registers should only be used for any routine polling of the channel's status. Likewise, the Ch X Interrupt Status registers should only be used for acquiring a channel's status during an interrupt routine. If there were only 1 channel status register, polling it just after an interrupt occurred, but before it could be read by the interrupt routine, could prematurely clear the status bit. This could mask the true cause of the interrupt.

A system or board level reset will clear all channel Interrupt Enable registers, as well as all channel Interrupt Status registers and all channel Polling Status registers. A channel reset will only clear the interrupt and status registers belonging to the channel.

Missing Readback Count Registers

Each channel has an 8-bit Missing Readback register. These Read Only registers are used to store the number of times no readbacks were returned from a PSI after a setpoint was sent to it. The format of the registers is shown below.

Missing Readback Register

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

Each channel has an 8-bit counter that keeps track of the number of missed readback occurrences. Any period between two setpoints without a PSI response of at least one readback is considered a missed readback occurrence.

The maximum value the counter will hold is 255. The LSB of the count is stored in bit D0 of the Missing Readback register. The MSB of the count is stored in bit D7 of the Missing Readback register. Upon reading the Missing Readback register, the counter will be cleared.

The addresses of each channel's Missing Readback register can be found in Appendix A and Appendix B.

BOARD AND CHANNEL RESETS

There are two ways to reset the V233 module. The first way is to manually issue a system reset by pushing the VME crate's reset button. This will reset the entire chassis as well as the V233. The second way is to issue a board reset command from the VME controller to the V233 module's System Reset register.

The System Reset register is an 8-bit Write Only register, automatically cleared after being written. The register is located at the A24 base addresses + 2Dh. The upper 7 bits of this register are not used. However, when a "1" is written to the lowest bit, D0, the V233 module will undergo a system reset. The bit is cleared automatically after the register is written.

In addition to a system reset, it is possible to reset the individual channels. The Ch 1 Reset register, Ch 2 Reset register, Ch 3 Reset register, and Ch 4 Reset register, are used to reset their own channel. These are 8-bit Write Only registers, and are automatically cleared after they are written. The address locations of these registers can be found in Appendix A and Appendix B. The upper 7 bits of these registers are not used. However, when a "1" is written to the lowest bit, D0, of a Ch X Reset register, the associated channel will be reset. The bit is cleared automatically after the register is written.

A board or channel reset takes about 160 microseconds to complete. Following a system or board reset, bit D11 of the Main Interrupt Status register and the Main Polling Status register will go low. Approximately 160 microseconds later, bit D11 will go high, indicating the board is ready for use. When a channel is reset, that channel also takes 160 microseconds to fully reset. However, there is no status bit to indicate when an individual channel is ready for use. The programmer should account for this when issuing a channel reset.

V233 Function Generator

A board reset issued to the V233 module will do the following:

- 1) Clear the Channel Arm Register (End all channel functions)
- 2) Re-initialize the VME interface
- 3) Restart the Event Link decoder
- 4) Clear Event Link Simulator registers
- 5) Clear the Page register
- 6) Clear any active interrupt
- 7) Clear the Interrupt Level register
- 8) Clear the Interrupt Vector register
- 9) Clear the Interrupt Enable register
- 10) Clear the low byte of Main Interrupt Status register
- 11) Clear the low byte of Main Polling Status register
- 12) Disable PPM (set board to user 1)
- 13) Clear the User Switch Code register
- 14) Clear the 8 User X Code registers
- 15) Clear the User History register
- 16) Re-initialize all channel DRAM (Data in DRAM not lost)
- 17) Re-initialize all channel DRAM interfaces
- 18) Clear all channel Interrupt Enable registers
- 19) Clear all channel Interrupt Status registers
- 20) Clear all channel Polling Status registers
- 21) Clear all channel Setpoint Count registers and counters
- 22) Re-initialize all channel Start, Resume, and Group End controls
- 23) Re-initialize all channel start and resume delay controls (Delays not lost)
- 24) Clear all channel Clock Select registers
- 25) Clear all channel Frame ID registers
- 26) Clear all channel Start Event registers
- 27) Clear all channel Resume Event 1 registers
- 28) Clear all channel Resume Event 2 registers
- 29) Clear all channel Resume Event 3 registers
- 30) Clear all channel Resume Event 4 registers
- 31) Clear all channel Group End Event registers
- 32) Clear all channel Tag Event registers
- 33) Clear all channel Switch Active Buffer registers
- 34) Clear Switch Buffer Ready register
- 35) Clear all channel Active Buffers registers
- 36) Clear all channel Missing Readback Counters
- 37) Re-initialize all channel setpoint controls
- 38) Re-initialize all channel readback controls
- 39) Restart all channel PSI encoders
- 40) Restart all channel PSI decoders

V233 Function Generator

A channel reset issued to the V233 module will do the following:

- 1) End channel function if currently active (Channel not dis-armed)
- 2) Re-initialize channel DRAM (Data in DRAM not lost)
- 3) Re-initialize channel DRAM interface
- 4) Clear channel Interrupt Enable register
- 5) Clear channel Interrupt Status register
- 6) Clear channel Polling Status register
- 7) Clear channel Setpoint Count registers and counter
- 8) Re-initialize channel Start, Resume, and Group End controls
- 9) Re-initialize channel start and resume delay controls (Delays not lost)
- 10) Clear channel Clock Select register
- 11) Clear channel Frame ID register
- 12) Clear channel Start Event register
- 13) Clear channel Resume Event 1 register
- 14) Clear channel Resume Event 2 register
- 15) Clear channel Resume Event 3 register
- 16) Clear channel Resume Event 4 register
- 17) Clear channel Group End Event register
- 18) Clear channel Tag Event register
- 19) Clear channel Switch Active Buffer registers
- 20) Clear channel Active Buffers register
- 21) Re-initialize channel setpoint controls
- 22) Re-initialize channel readback controls
- 23) Restart channel PSI encoder
- 24) Restart channel PSI decoder
- 25) Clear channel Command ID register
- 26) Clear channel Command register
- 27) Clear channel Readback ID registers
- 28) Clear channel Readback Data registers
- 29) Clear channel Readback Count register
- 30) Clear channel command controls
- 31) Clear channel Missing Readback Counter

Note that a reset will not cause the on-board DRAM (setpoints and readbacks) to lose its contents. Nor will a reset cause any start delay or resume delay values to be lost from the Dual Port RAM located in each of the channel's FPGAs.

GROUNDING JUMPERS

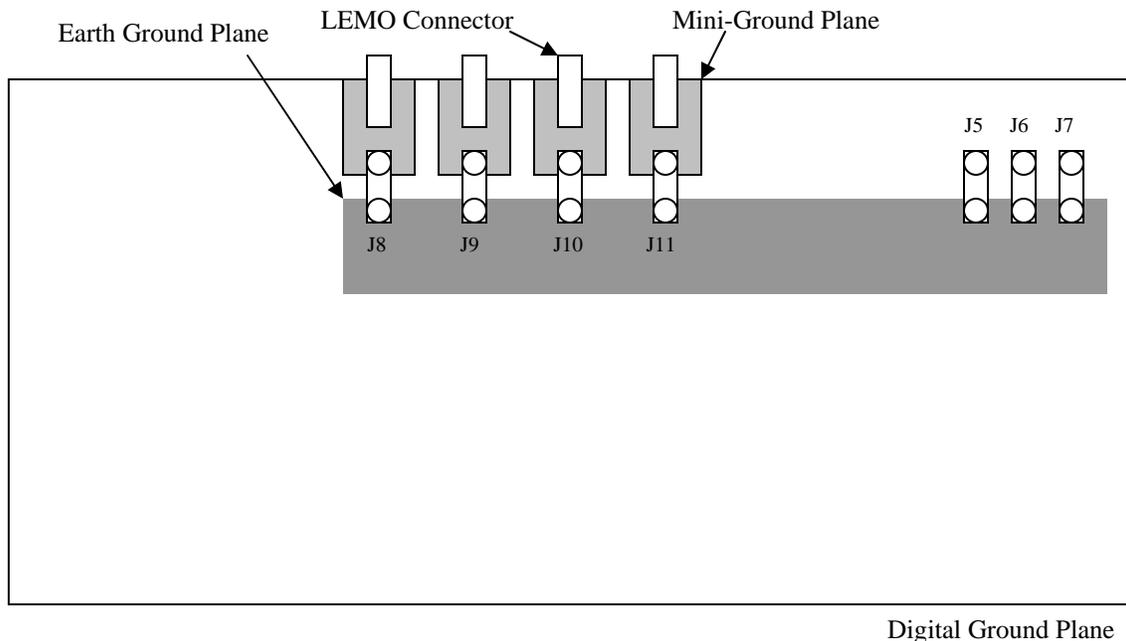
The V233 module is a 10-layer board. Layer 5 is the digital ground plane, used as the primary ground for all on-board digital logic. The digital ground plane is connected to the VME ground through 39 pins, spread out over backplane connectors P1 and P2.

In addition to the digital ground plane, there is a very small earth ground plane, found on layer 2. This earth ground plane is connected to pins C1, C2, C3, C4, C5, and C6, of connector P2, which are user-defined pins. There are also 4 mini-ground planes, 1 dedicated to each of the 4 LEMO input connectors on the front panel. These mini-ground planes, separate from each other, are found on layer 3, close to the connectors.

Each of the 4 LEMO connectors has its shell tied directly to its own mini-ground plane. Each of the 4 mini-ground planes is capacitively coupled to the earth ground plane, which is roughly the size of the 4 mini-ground planes combined. Each mini-ground plane has a dedicated jumper, providing a means to short the coupling capacitor, directly connecting the mini-ground plane to the earth ground plane. J11 shorts the Gauss Clock connector's mini-ground plane to the earth ground plane. J10 shorts the Start connector's mini-ground plane to the earth ground plane. J9 shorts the Resume connector's mini-ground plane to the earth ground plane. J8 shorts the Group End connector's mini-ground plane to the earth ground plane.

As an added option, the earth ground plane has 3 dedicated jumpers, J5, J6, and J7, which can be used to short the earth ground plane to the digital ground plane.

The Function Generator's default configuration has J5, J6, and J7 jumped, and J8, J9, J10, and J11 left open. Below is a representative drawing of the ground planes and their jumpers.



REVISIONS

This manual was written for Revision “B” of the V233 programmed assembly module. It supercedes all others written prior to 1/30/08.

APPENDIX A

V233 Register and Memory Assignments

TABLE OF CONTENTS

Abbreviation Key.....	Page 3
VME ID Registers.....	Page 4
Page Register.....	Page 4
Global Interrupt And Status Registers.....	Page 4
System Reset Register.....	Page 4
Channel Arm Register.....	Page 5
Event Link Simulator Registers.....	Page 5
Switch Buffer Ready Register.....	Page 5
User Control Registers.....	Page 5
A32 Address Map Register.....	Page 5
Channel 1 Interrupt And Status Registers.....	Page 6
Channel 1 Reset Register.....	Page 6
Channel 1 VME Commands Register.....	Page 6
Channel 1 Clock Select Register.....	Page 6
Channel 1 Missing Readback Count Register.....	Page 6
Channel 1 Active Buffers Register.....	Page 7
Channel 1 Setpoint Count Registers.....	Page 7
Channel 1 Frame ID Register.....	Page 7
Channel 1 Event Registers.....	Page 7
Channel 1 User Switch Active Buffer Registers.....	Page 8
Channel 1 Start Delay Registers.....	Page 8
Channel 1 Resume 1 Delay Registers.....	Page 9
Channel 1 Resume 2 Delay Registers.....	Page 9
Channel 1 Resume 3 Delay Registers.....	Page 10
Channel 1 Resume 4 Delay Registers.....	Page 10
Channel 1 Single Frame Registers.....	Page 11
Channel 2 Interrupt And Status Registers.....	Page 12
Channel 2 Reset Register.....	Page 12
Channel 2 VME Commands Register.....	Page 12
Channel 2 Clock Select Register.....	Page 12
Channel 2 Missing Readback Count Register.....	Page 12
Channel 2 Active Buffers Register.....	Page 13
Channel 2 Setpoint Count Registers.....	Page 13
Channel 2 Frame ID Register.....	Page 13
Channel 2 Event Registers.....	Page 13
Channel 2 User Switch Active Buffer Registers.....	Page 14

Appendix A - V233 Register Assignments

Channel 2 Start Delay Registers.....	Page 14
Channel 2 Resume 1 Delay Registers.....	Page 15
Channel 2 Resume 2 Delay Registers.....	Page 15
Channel 2 Resume 3 Delay Registers.....	Page 16
Channel 2 Resume 4 Delay Registers.....	Page 16
Channel 2 Single Frame Registers.....	Page 17
Channel 3 Interrupt And Status Registers.....	Page 18
Channel 3 Reset Register.....	Page 18
Channel 3 VME Commands Register.....	Page 18
Channel 3 Clock Select Register.....	Page 18
Channel 3 Missing Readback Count Register.....	Page 18
Channel 3 Active Buffers Register.....	Page 19
Channel 3 Setpoint Count Registers.....	Page 19
Channel 3 Frame ID Register.....	Page 19
Channel 3 Event Registers.....	Page 19
Channel 3 User Switch Active Buffer Registers.....	Page 20
Channel 3 Start Delay Registers.....	Page 20
Channel 3 Resume 1 Delay Registers.....	Page 21
Channel 3 Resume 2 Delay Registers.....	Page 21
Channel 3 Resume 3 Delay Registers.....	Page 22
Channel 3 Resume 4 Delay Registers.....	Page 22
Channel 3 Single Frame Registers.....	Page 23
Channel 4 Interrupt And Status Registers.....	Page 24
Channel 4 Reset Register.....	Page 24
Channel 4 VME Commands Register.....	Page 24
Channel 4 Clock Select Register.....	Page 24
Channel 4 Missing Readback Count Register.....	Page 24
Channel 4 Active Buffers Register.....	Page 25
Channel 4 Setpoint Count Registers.....	Page 25
Channel 4 Frame ID Register.....	Page 25
Channel 4 Event Registers.....	Page 25
Channel 4 User Switch Active Buffer Registers.....	Page 26
Channel 4 Start Delay Registers.....	Page 26
Channel 4 Resume 1 Delay Registers.....	Page 27
Channel 4 Resume 2 Delay Registers.....	Page 27
Channel 4 Resume 3 Delay Registers.....	Page 28
Channel 4 Resume 4 Delay Registers.....	Page 28
Channel 4 Single Frame Registers.....	Page 29

Appendix A - V233 Register Assignments

Abbreviation Key

Characters enclosed in quotes (“ ”) are ASCII characters

x = “Don’t Care” bit

z = Bit does not exist

? = Programmable bit

* = Programmable bit

\$ = Programmable bit

THO = Thousands

HUN = Hundreds

TEN = Tens

UNIT = Units

RO = Read Only

RW = Read/Write

ROAC = Read Only/Automatic Clear

WOAC = Write Only/Automatic Clear

ROWTC = Read Only/Write To Clear

RWAC = Read/Write/Automatic Clear

Appendix A - V233 Register Assignments

VME ID Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0000h	VME ID	RO	“V”	“M”	V = 56h; M = 4Dh
0002h	VME ID	RO	“E”	“I”	E = 45h; I = 49h
0004h	VME ID	RO	“D”	“B”	D = 44h; B = 42h
0006h	VME ID	RO	“N”	“L”	N = 46h; L = 4Ch
0008h	VME ID	RO	“V”	“2”	V = 56h; 1 = 32h
000Ah	VME ID	RO	“3”	“3”	3 = 33h; 3 = 33h
000Ch	VME ID	RO	00h	00h	All zeros
000Eh	VME ID	RO	“R”	“E”	R = 52h; E = 45h
0010h	VME ID	RO	“V”	Letter	V = 56h; Letter = A...H
0012h	VME ID	RO	00h	00h	All zeros
0014h	VME ID	RO	“S”	“E”	S = 53h; E = 45h
0016h	VME ID	RO	“R”	“#”	R = 52h; # = 23h
0018h	VME ID	RO	THO	HUN	THO = 0; HUN = 0...2
001Ah	VME ID	RO	TEN	UNIT	TEN = 0...9; UNIT = 0...9
001Ch	VME ID	RO	00h	00h	All zeros
001Eh	VME ID	RO	00h	00h	All zeros

Page Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0020h	DRAM Paging	RW	xxxxxxx?	????????	D8...D0 determine DRAM page

Global Interrupt And Status Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0022h	Interrupt Level	RW	zzzzzzzz	xxxxx???	00h disables all interrupts
0024h	Interrupt Vector	RW	????????	????????	Status/ID response
0026h	Interrupt Enable	RW	zzzzzzzz	????x???	1 enables interrupt; 0 disables interrupt
0028h	Main Interrupt Status	ROAC	0000\$***	????????	\$ = Board ready; *** = User code; ???????? = Status bits
002Ah	Main Polling Status	ROAC	0000\$***	????????	\$ = Board ready; *** = User code; ???????? = Status bits

System Reset Register

VME Offset	Purpose	Access	High Byte	Low Byte	
002Ch	Board Reset	WOAC	zzzzzzzz	zzzzzzz?	Set D0 to reset board; Auto clears

Appendix A - V233 Register Assignments

Channel Arm Register

VME Offset	Purpose	Access	High Byte	Low Byte	
002Eh	Arm Channels	RW	ZZZZZZZ	xxxx????	Set D0...D3 to arm channels 1...4

Event Link Simulator Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0030h	Simulated Event	RW	ZZZZZZZ	????????	D7...D0 = Simulated Event Link word
0032h	Simulator Control	RW	ZZZZZZZ	xxxxx*?	? = 1 = Simulator Mode; * = 1 = Send word; Auto clears

Switch Buffer Ready Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0034h	Switch Buffer Code	RW	xxxxxxx*	????????	* = Switch Buffer active; ???????? = event

User Control Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0040h	User Switch Code	RW	xxxxxxx*	????????	* = PPM active; ???????? = event
0042h	User 1 Code	RW	xxxxxxx*	????????	* = User 1 active; ???????? = event
0044h	User 2 Code	RW	xxxxxxx*	????????	* = User 2 active; ???????? = event
0046h	User 3 Code	RW	xxxxxxx*	????????	* = User 3 active; ???????? = event
0048h	User 4 Code	RW	xxxxxxx*	????????	* = User 4 active; ???????? = event
004Ah	User 5 Code	RW	xxxxxxx*	????????	* = User 5 active; ???????? = event
004Ch	User 6 Code	RW	xxxxxxx*	????????	* = User 6 active; ???????? = event
004Eh	User 7 Code	RW	xxxxxxx*	????????	* = User 7 active; ???????? = event
0050h	User 8 Code	RW	xxxxxxx*	????????	* = User 8 active; ???????? = event
0052h	User History	ROWTC	ZZZZZZZ	????????	???????? = User 8...1 was active

A32 Address Map Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0060h	A32 Base Address	RO	000000??	????????	???????? = 10-bit A32 base address

Appendix A - V233 Register Assignments

Channel 1 Interrupt And Status Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0800h	Ch 1 Interrupt Enable	RW	????????	???xx???	1 enables interrupt; 0 disables interrupt
0802h	Ch 1 Interrupt Status	ROAC	????????	????????	???????? = Status bits
0804h	Ch 1 Polling Status	ROAC	????????	????????	???????? = Status bits

Channel 1 Reset Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0806h	Reset Chan 1	WOAC	zzzzzzzz	zzzzzzz?	Set D0 to reset channel 1; Auto clears

Channel 1 VME Commands Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0808h	Issue VME Start, Resume, Group End, or Tag Command	WOAC	zzzzzzzz	zzzz????	Set D0 to issue Start command Set D1 to issue Resume 1 command Set D2 to issue Group End command Set D3 to issue Tag command

Channel 1 Clock Select Register

VME Offset	Purpose	Access	High Byte	Low Byte	
080Ah	Clock And External Input Selection	RW	zzzzzzzz	????????	Set D7...D0 to select setpoint clock and to activate external inputs

Channel 1 Missing Readback Register

VME Offset	Purpose	Access	High Byte	Low Byte	
080Ch	Ch 1 Missing Readback Count	ROAC	zzzzzzzz	????????	???????? = Missing Readback Count

Appendix A - V233 Register Assignments

Channel 1 Active Buffers Register

VME Offset	Purpose	Access	High Byte	Low Byte	
080Eh	Chan 1 Active Buffers	RO	xxxxxxx*	????????	* = Active Readback buffer; D7...D0 = Active user 8...1 setpoint buffers

Channel 1 Setpoint Count Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0810h	Ch 1 Setpoint Count High	RO	zzzzzzzz	????????	D7...D0 = High byte of setpoint count
0812h	Ch 1 Setpoint Count Low	RO	????????	????????	D15...D0 = Low bytes of setpoint count

Channel 1 Frame ID Register

VME Offset	Purpose	Access	High Byte	Low Byte	
0814h	Ch 1 Frame ID	RW	zzzzzzzz	????????	???????? = PSI Frame ID

Channel 1 Event Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0820h	Ch 1 Start Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
0822h	Ch 1 Resume 1 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
0824h	Ch 1 Resume 2 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
0826h	Ch 1 Resume 3 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
0828h	Ch 1 Resume 4 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
082Ah	Ch 1 Group End Event	RW	xx^^^\$\$*	????????	* = Event active; ???????? = event; ^^^ = User; \$\$ = Halt control bits
082C	Ch Tag Event	RW	xxxxxxx#*	????????	# = Use external tag input; * = Event active; ???????? = event

Appendix A - V233 Register Assignments

Channel 1 User Switch Active Buffer Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0830h	Switch User 1 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 1 setpoint buffers at Group End event
0832h	Switch User 2 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 2 setpoint buffers at Group End event
0834h	Switch User 2 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 3 setpoint buffers at Group End event
0836h	Switch User 4 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 4 setpoint buffers at Group End event
0838h	Switch User 5 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 5 setpoint buffers at Group End event
083Ah	Switch User 6 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 6 setpoint buffers at Group End event
083Ch	Switch User 7 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 7 setpoint buffers at Group End event
083Eh	Switch User 8 setpoint buffer	WOAC	ZZZZZZL	ZZZZZZ?	? = 1 = Switch User 8 setpoint buffers at Group End event

Channel 1 Start Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0840h	U1 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
0842h	U1 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
0844h	U2 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
0846h	U2 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
0848h	U3 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
084Ah	U3 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
084Ch	U4 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
084Eh	U4 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
0850h	U5 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
0852h	U5 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
0854h	U6 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
0856h	U6 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
0858h	U7 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
085Ah	U7 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0
085Ch	U8 Strt Dly Hi	RW	ZZZZZZL	???????	??????? = Delay bits 23...16
085Eh	U8 Strt Dly Lo	RW	???????	???????	??????? ??????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 1 Resume 1 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0860h	U1 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0862h	U1 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0864h	U2 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0866h	U2 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0868h	U3 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
086Ah	U3 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
086Ch	U4 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
086Eh	U4 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0870h	U5 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0872h	U5 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0874h	U6 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0876h	U6 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0878h	U7 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
087Ah	U7 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
087Ch	U8 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
087Eh	U8 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Channel 1 Resume 2 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
0880h	U1 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0882h	U1 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0884h	U2 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0886h	U2 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0888h	U3 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
088Ah	U3 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
088Ch	U4 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
088Eh	U4 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0890h	U5 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0892h	U5 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0894h	U6 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
0896h	U6 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
0898h	U7 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
089Ah	U7 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
089Ch	U8 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
089Eh	U8 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 1 Resume 3 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
08A0h	U1 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08A2h	U1 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08A4h	U2 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08A6h	U2 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08A8h	U3 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08AAh	U3 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08ACh	U4 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08AEh	U4 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08B0h	U5 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08B2h	U5 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08B4h	U6 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08B6h	U6 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08B8h	U7 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08BAh	U7 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08BCh	U8 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08BEh	U8 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Channel 1 Resume 4 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
08C0h	U1 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08C2h	U1 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08C4h	U2 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08C6h	U2 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08C8h	U3 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08CAh	U3 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08CCh	U4 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08CEh	U4 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08D0h	U5 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08D2h	U5 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08D4h	U6 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08D6h	U6 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08D8h	U7 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08DAh	U7 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
08DCh	U8 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
08DEh	U8 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 1 Single Frame Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
08E0h	Single Frame ID	RW	*****	???????	* = Aux Bits; ? = Frame ID
08E2h	Single Frame Data Field	RW	???????	???????	?????? ???? = Data bits
08E4h	Readback ID 1	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 1
08E6h	Readback 1	RO	???????	???????	?????? ???? = Readback 1
08E8h	Readback ID 2	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 2
08EAh	Readback 2	RO	???????	???????	?????? ???? = Readback 2
08ECh	Readback ID 3	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 3
08EEh	Readback 3	RO	???????	???????	?????? ???? = Readback 3
08F0h	Readback ID 4	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 4
08F2h	Readback 4	RO	???????	???????	?????? ???? = Readback 4
08F4h	Readback ID 5	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 5
08F6h	Readback 5	RO	???????	???????	?????? ???? = Readback 5
08F8h	Readback ID 6	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 6
08FAh	Readback 6	RO	???????	???????	?????? ???? = Readback 6
08FCh	Send Single Frame	RWAC	ZZZZZZ	xxxxx???	D0 = Send frame when armed; D1 = Send frame at Group End; D1 = Inhibit Timing Trigger update
08FEh	Readback Count	RO	ZZZZZZ	xxxxx???	??? = Readback count; Cleared when frame sent

Appendix A - V233 Register Assignments

Channel 2 Interrupt And Status Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1000h	Ch 2 Interrupt Enable	RW	????????	???xx???	1 enables interrupt; 0 disables interrupt
1002h	Ch 2 Interrupt Status	ROAC	????????	????????	???????? = Status bits
1004h	Ch 2 Polling Status	ROAC	????????	????????	???????? = Status bits

Channel 2 Reset Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1006h	Reset Chan 2	WOAC	zzzzzzzz	zzzzzzz?	Set D0 to reset channel 1; Auto clears

Channel 2 VME Commands Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1008h	Issue VME Start, Resume, Group End, or Tag Command	WOAC	zzzzzzzz	zzzz????	Set D0 to issue Start command Set D1 to issue Resume 1 command Set D2 to issue Group End command Set D3 to issue Tag command

Channel 2 Clock Select Register

VME Offset	Purpose	Access	High Byte	Low Byte	
100Ah	Clock And External Input Selection	RW	zzzzzzzz	????????	Set D7...D0 to select setpoint clock and to activate external inputs

Channel 2 Missing Readback Register

VME Offset	Purpose	Access	High Byte	Low Byte	
100Ch	Ch 2 Missing Readback Count	ROAC	zzzzzzzz	????????	???????? = Missing Readback Count

Appendix A - V233 Register Assignments

Channel 2 Active Buffers Register

VME Offset	Purpose	Access	High Byte	Low Byte	
100Eh	Chan 2 Active Buffers	RO	xxxxxxx*	????????	* = Active Readback buffer; D7...D0 = Active user 8...1 setpoint buffers

Channel 2 Setpoint Count Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1010h	Ch 2 Setpoint Count High	RO	zzzzzzzz	????????	D7...D0 = High byte of setpoint count
1012h	Ch 2 Setpoint Count Low	RO	????????	????????	D15...D0 = Low bytes of setpoint count

Channel 2 Frame ID Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1014h	Ch 2 Frame ID	RW	zzzzzzzz	????????	???????? = PSI Frame ID

Channel 2 Event Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1020h	Ch 2 Start Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1022h	Ch 2 Resume 1 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1024h	Ch 2 Resume 2 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1026h	Ch 2 Resume 3 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1028h	Ch 2 Resume 4 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
102Ah	Ch 2 Group End Event	RW	xxxxx\$\$*	????????	* = Event active; ???????? = event; \$\$ = Halt control bits
102Ch	Ch 2 Tag Event	RW	xx^^^\$\$*	????????	* = Event active; ???????? = event; ^^^ = User; \$\$ = Halt control bits

Appendix A - V233 Register Assignments

Channel 2 User Switch Active Buffer Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1030h	Switch User 1 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 1 setpoint buffers at Group End event
1032h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 2 setpoint buffers at Group End event
1034h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 3 setpoint buffers at Group End event
1036h	Switch User 4 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 4 setpoint buffers at Group End event
1038h	Switch User 5 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 5 setpoint buffers at Group End event
103Ah	Switch User 6 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 6 setpoint buffers at Group End event
103Ch	Switch User 7 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 7 setpoint buffers at Group End event
103Eh	Switch User 8 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 8 setpoint buffers at Group End event

Channel 2 Start Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1040h	U1 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1042h	U1 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1044h	U2 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1046h	U2 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1048h	U3 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
104Ah	U3 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
104Ch	U4 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
104Eh	U4 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1050h	U5 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1052h	U5 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1054h	U6 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1056h	U6 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1058h	U7 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
105Ah	U7 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
105Ch	U8 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
105Eh	U8 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 2 Resume 1 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1060h	U1 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1062h	U1 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1064h	U2 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1066h	U2 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1068h	U3 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
106Ah	U3 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
106Ch	U4 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
106Eh	U4 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1070h	U5 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1072h	U5 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1074h	U6 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1076h	U6 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1078h	U7 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
107Ah	U7 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
107Ch	U8 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
107Eh	U8 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Channel 2 Resume 2 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1080h	U1 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1082h	U1 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1084h	U2 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1086h	U2 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1088h	U3 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
108Ah	U3 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
108Ch	U4 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
108Eh	U4 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1090h	U5 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1092h	U5 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1094h	U6 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1096h	U6 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1098h	U7 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
109Ah	U7 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
109Ch	U8 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
109Eh	U8 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 2 Resume 3 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
10A0h	U1 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10A2h	U1 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10A4h	U2 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10A6h	U2 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10A8h	U3 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10AAh	U3 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10ACh	U4 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10AEh	U4 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10B0h	U5 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10B2h	U5 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10B4h	U6 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10B6h	U6 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10B8h	U7 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10BAh	U7 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10BCh	U8 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10BEh	U8 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0

Channel 2 Resume 4 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
10C0h	U1 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10C2h	U1 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10C4h	U2 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10C6h	U2 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10C8h	U3 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10CAh	U3 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10CCh	U4 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10CEh	U4 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10D0h	U5 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10D2h	U5 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10D4h	U6 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10D6h	U6 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10D8h	U7 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10DAh	U7 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
10DCh	U8 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
10DEh	U8 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 2 Single Frame Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
10E0h	Single Frame ID	RW	*****	???????	* = Aux Bits; ? = Frame ID
10E2h	Single Frame Data Field	RW	???????	???????	?????? ???? = Data bits
10E4h	Readback ID 1	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 1
10E6h	Readback 1	RO	???????	???????	?????? ???? = Readback 1
10E8h	Readback ID 2	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 2
10EAh	Readback 2	RO	???????	???????	?????? ???? = Readback 2
10ECh	Readback ID 3	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 3
10EEh	Readback 3	RO	???????	???????	?????? ???? = Readback 3
10F0h	Readback ID 4	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 4
10F2h	Readback 4	RO	???????	???????	?????? ???? = Readback 4
10F4h	Readback ID 5	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 5
10F6h	Readback 5	RO	???????	???????	?????? ???? = Readback 5
10F8h	Readback ID 6	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 6
10FAh	Readback 6	RO	???????	???????	?????? ???? = Readback 6
10FCh	Send Single Frame	RWAC	ZZZZZZZ	xxxxx???	D0 = Send frame when armed; D1 = Send frame at Group End; D1 = Inhibit Timing Trigger update
10FEh	Readback Count	RO	ZZZZZZZ	xxxxx???	??? = Readback count; Cleared when frame sent

Appendix A - V233 Register Assignments

Channel 3 Interrupt And Status Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1800h	Ch 3 Interrupt Enable	RW	????????	???xx???	1 enables interrupt; 0 disables interrupt
1802h	Ch 3 Interrupt Status	ROAC	????????	????????	???????? = Status bits
1804h	Ch 3 Polling Status	ROAC	????????	????????	???????? = Status bits

Channel 3 Reset Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1806h	Reset Chan 3	WOAC	zzzzzzzz	zzzzzzz?	Set D0 to reset channel 1; Auto clears

Channel 3 VME Commands Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1808h	Issue VME Start, Resume, Group End, Or Tag Command	WOAC	zzzzzzzz	zzzz????	Set D0 to issue Start command Set D1 to issue Resume 1 command Set D2 to issue Group End command Set D3 to issue Tag command

Channel 3 Clock Select Register

VME Offset	Purpose	Access	High Byte	Low Byte	
180Ah	Clock And External Input Selection	RW	zzzzzzzz	????????	Set D7...D0 to select setpoint clock and to activate external inputs

Channel 3 Missing Readback Register

VME Offset	Purpose	Access	High Byte	Low Byte	
180Ch	Ch 3 Missing Readback Count	ROAC	zzzzzzzz	????????	???????? = Missing Readback Count

Appendix A - V233 Register Assignments

Channel 3 Active Buffers Register

VME Offset	Purpose	Access	High Byte	Low Byte	
180Eh	Chan 3 Active Buffers	RO	xxxxxxx*	????????	* = Active Readback buffer; D7...D0 = Active user 8...1 setpoint buffers

Channel 3 Setpoint Count Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1810h	Ch 3 Setpoint Count High	RO	zzzzzzzz	????????	D7...D0 = High byte of setpoint count
1812h	Ch 3 Setpoint Count Low	RO	????????	????????	D15...D0 = Low bytes of setpoint count

Channel 3 Frame ID Register

VME Offset	Purpose	Access	High Byte	Low Byte	
1814h	Ch 3 Frame ID	RW	zzzzzzzz	????????	???????? = PSI Frame ID

Channel 3 Event Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1820h	Ch 3 Start Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1822h	Ch 3 Resume 1 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1824h	Ch 3 Resume 2 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1826h	Ch 3 Resume 3 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
1828h	Ch 3 Resume 4 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
182Ah	Ch 3 Group End Event	RW	xx^^^\$\$*	????????	* = Event active; ???????? = event; ^^^ = User; \$\$ = Halt control bits
182Ch	Ch 3 Tag Event	RW	xxxxxxx#*	????????	# = Use external tag input; * = Event active; ???????? = event

Appendix A - V233 Register Assignments

Channel 3 User Switch Active Buffer Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1830h	Switch User 1 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 1 setpoint buffers at Group End event
1832h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 2 setpoint buffers at Group End event
1834h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 3 setpoint buffers at Group End event
1836h	Switch User 4 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 4 setpoint buffers at Group End event
1838h	Switch User 5 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 5 setpoint buffers at Group End event
183Ah	Switch User 6 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 6 setpoint buffers at Group End event
183Ch	Switch User 7 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 7 setpoint buffers at Group End event
183Eh	Switch User 8 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 8 setpoint buffers at Group End event

Channel 3 Start Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1840h	U1 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1842h	U1 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1844h	U2 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1846h	U2 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1848h	U3 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
184Ah	U3 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
184Ch	U4 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
184Eh	U4 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1850h	U5 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1852h	U5 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1854h	U6 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1856h	U6 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
1858h	U7 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
185Ah	U7 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
185Ch	U8 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
185Eh	U8 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 3 Resume 1 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1860h	U1 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1862h	U1 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1864h	U2 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1866h	U2 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1868h	U3 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
186Ah	U3 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
186Ch	U4 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
186Eh	U4 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1870h	U5 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1872h	U5 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1874h	U6 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1876h	U6 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1878h	U7 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
187Ah	U7 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
187Ch	U8 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
187Eh	U8 R1 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Channel 3 Resume 2 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
1880h	U1 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1882h	U1 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1884h	U2 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1886h	U2 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1888h	U3 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
188Ah	U3 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
188Ch	U4 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
188Eh	U4 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1890h	U5 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1892h	U5 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1894h	U6 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
1896h	U6 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
1898h	U7 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
189Ah	U7 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
189Ch	U8 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
189Eh	U8 R2 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 3 Resume 3 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
18A0h	U1 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18A2h	U1 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18A4h	U2 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18A6h	U2 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18A8h	U3 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18AAh	U3 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18ACh	U4 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18AEh	U4 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18B0h	U5 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18B2h	U5 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18B4h	U6 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18B6h	U6 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18B8h	U7 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18BAh	U7 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18BCh	U8 R3 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18BEh	U8 R3 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0

Channel 3 Resume 4 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
18C0h	U1 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18C2h	U1 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18C4h	U2 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18C6h	U2 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18C8h	U3 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18CAh	U3 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18CCh	U4 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18CEh	U4 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18D0h	U5 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18D2h	U5 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18D4h	U6 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18D6h	U6 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18D8h	U7 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18DAh	U7 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0
18DCh	U8 R4 Dly Hi	RW	ZZZZZZZ	???????	?????? = Delay bits 23...16
18DEh	U8 R4 Dly Lo	RW	???????	???????	?????? ???? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 3 Single Frame Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
18E0h	Single Frame ID	RW	*****	???????	* = Aux Bits; ? = Frame ID
18E2h	Single Frame Data Field	RW	???????	???????	?????? ???? = Data bits
18E4h	Readback ID 1	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 1
18E6h	Readback 1	RO	???????	???????	?????? ???? = Readback 1
18E8h	Readback ID 2	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 2
18EAh	Readback 2	RO	???????	???????	?????? ???? = Readback 2
18ECh	Readback ID 3	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 3
18EEh	Readback 3	RO	???????	???????	?????? ???? = Readback 3
18F0h	Readback ID 4	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 4
18F2h	Readback 4	RO	???????	???????	?????? ???? = Readback 4
18F4h	Readback ID 5	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 5
18F6h	Readback 5	RO	???????	???????	?????? ???? = Readback 5
18F8h	Readback ID 6	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 6
18FAh	Readback 6	RO	???????	???????	?????? ???? = Readback 6
18FCh	Send Single Frame	RWAC	ZZZZZZ	xxxxx???	D0 = Send frame when armed; D1 = Send frame at Group End; D1 = Inhibit Timing Trigger update
18FEh	Readback Count	RO	ZZZZZZ	xxxxx???	??? = Readback count; Cleared when frame sent

Appendix A - V233 Register Assignments

Channel 4 Interrupt And Status Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2000h	Ch 4 Interrupt Enable	RW	????????	???xx???	1 enables interrupt; 0 disables interrupt
2002h	Ch 4 Interrupt Status	ROAC	????????	????????	???????? = Status bits
2004h	Ch 4 Polling Status	ROAC	????????	????????	???????? = Status bits

Channel 4 Reset Register

VME Offset	Purpose	Access	High Byte	Low Byte	
2006h	Reset Chan 4	WOAC	zzzzzzzz	zzzzzzz?	Set D0 to reset channel 1; Auto clears

Channel 4 VME Commands Register

VME Offset	Purpose	Access	High Byte	Low Byte	
2008h	Issue VME Start, Resume, Group End, Or Tag Command	WOAC	zzzzzzzz	zzzz????	Set D0 to issue Start command Set D1 to issue Resume 1 command Set D2 to issue Group End command Set D3 to issue Tag command

Channel 4 Clock Select Register

VME Offset	Purpose	Access	High Byte	Low Byte	
200Ah	Clock And External Input Selection	RW	zzzzzzzz	????????	Set D7...D0 to select setpoint clock and to activate external inputs

Channel 4 Missing Readback Register

VME Offset	Purpose	Access	High Byte	Low Byte	
200Ch	Ch 4 Missing Readback Count	ROAC	zzzzzzzz	????????	???????? = Missing Readback Count

Appendix A - V233 Register Assignments

Channel 4 Active Buffers Register

VME Offset	Purpose	Access	High Byte	Low Byte	
200Eh	Chan 4 Active Buffers	RO	xxxxxxx*	????????	* = Active Readback buffer; D7...D0 = Active user 8...1 setpoint buffers

Channel 4 Setpoint Count Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2010h	Ch 4 Setpoint Count High	RO	zzzzzzzz	????????	D7...D0 = High byte of setpoint count
2012h	Ch 4 Setpoint Count Low	RO	????????	????????	D15...D0 = Low bytes of setpoint count

Channel 4 Frame ID Register

VME Offset	Purpose	Access	High Byte	Low Byte	
2014h	Ch 4 Frame ID	RW	zzzzzzzz	????????	???????? = PSI Frame ID

Channel 4 Event Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2020h	Ch 4 Start Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
2022h	Ch 4 Resume 1 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
2024h	Ch 4 Resume 2 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
2026h	Ch 4 Resume 3 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
2028h	Ch 4 Resume 4 Event	RW	xxxxxxx*	????????	* = Event active; ???????? = event
202Ah	Ch 4 Group End Event	RW	xx^^^\$\$*	????????	* = Event active; ???????? = event; ^^^ = User; \$\$ = Halt control bits
202Ch	Ch 4 Tag Event	RW	xxxxxxx#*	????????	# = Use external tag input; * = Event active; ???????? = event

Appendix A - V233 Register Assignments

Channel 4 User Switch Active Buffer Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2030h	Switch User 1 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 1 setpoint buffers at Group End event
2032h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 2 setpoint buffers at Group End event
2034h	Switch User 2 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 3 setpoint buffers at Group End event
2036h	Switch User 4 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 4 setpoint buffers at Group End event
2038h	Switch User 5 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 5 setpoint buffers at Group End event
203Ah	Switch User 6 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 6 setpoint buffers at Group End event
203Ch	Switch User 7 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 7 setpoint buffers at Group End event
203Eh	Switch User 8 setpoint buffer	WOAC	ZZZZZZZZ	ZZZZZZZ?	? = 1 = Switch User 8 setpoint buffers at Group End event

Channel 4 Start Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2040h	U1 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2042h	U1 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
2044h	U2 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2046h	U2 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
2048h	U3 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
204Ah	U3 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
204Ch	U4 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
204Eh	U4 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
2050h	U5 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2052h	U5 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
2054h	U6 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2056h	U6 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
2058h	U7 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
205Ah	U7 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0
205Ch	U8 Strt Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
205Eh	U8 Strt Dly Lo	RW	????????	????????	???????? ???? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 4 Resume 1 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2060h	U1 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2062h	U1 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2064h	U2 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2066h	U2 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2068h	U3 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
206Ah	U3 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
206Ch	U4 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
206Eh	U4 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2070h	U5 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2072h	U5 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2074h	U6 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2076h	U6 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2078h	U7 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
207Ah	U7 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
207Ch	U8 R1 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
207Eh	U8 R1 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0

Channel 4 Resume 2 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
2080h	U1 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2082h	U1 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2084h	U2 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2086h	U2 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2088h	U3 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
208Ah	U3 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
208Ch	U4 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
208Eh	U4 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2090h	U5 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2092h	U5 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2094h	U6 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
2096h	U6 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
2098h	U7 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
209Ah	U7 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0
209Ch	U8 R2 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
209Eh	U8 R2 Dly Lo	RW	????????	????????	???????? ???????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 4 Resume 3 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
20A0h	U1 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20A2h	U1 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20A4h	U2 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20A6h	U2 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20A8h	U3 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20AAh	U3 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20ACh	U4 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20AEh	U4 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20B0h	U5 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20B2h	U5 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20B4h	U6 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20B6h	U6 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20B8h	U7 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20BAh	U7 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20BCh	U8 R3 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20BEh	U8 R3 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Channel 4 Resume 4 Delay Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
20C0h	U1 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20C2h	U1 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20C4h	U2 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20C6h	U2 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20C8h	U3 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20CAh	U3 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20CCh	U4 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20CEh	U4 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20D0h	U5 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20D2h	U5 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20D4h	U6 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20D6h	U6 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20D8h	U7 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20DAh	U7 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0
20DCh	U8 R4 Dly Hi	RW	ZZZZZZZZ	????????	???????? = Delay bits 23...16
20DEh	U8 R4 Dly Lo	RW	????????	????????	???????? ?????????? = Delay bits 15...0

Appendix A - V233 Register Assignments

Channel 4 Single Frame Registers

VME Offset	Purpose	Access	High Byte	Low Byte	
20E0h	Single Frame ID	RW	*****	???????	* = Aux Bits; ? = Frame ID
20E2h	Single Frame Data Field	RW	???????	???????	?????? ???? = Data bits
20E4h	Readback ID 1	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 1
20E6h	Readback 1	RO	???????	???????	?????? ???? = Readback 1
20E8h	Readback ID 2	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 2
20EAh	Readback 2	RO	???????	???????	?????? ???? = Readback 2
20ECh	Readback ID 3	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 3
20EEh	Readback 3	RO	???????	???????	?????? ???? = Readback 3
20F0h	Readback ID 4	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 4
20F2h	Readback 4	RO	???????	???????	?????? ???? = Readback 4
20F4h	Readback ID 5	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 5
20F6h	Readback 5	RO	???????	???????	?????? ???? = Readback 5
20F8h	Readback ID 6	RO	#####*	???????	# = Aux; * = CRC; ? = Readback ID 6
20FAh	Readback 6	RO	???????	???????	?????? ???? = Readback 6
20FCh	Send Single Frame	RWAC	ZZZZZZ	xxxxx???	D0 = Send frame when armed; D1 = Send frame at Group End; D1 = Inhibit Timing Trigger update
20FEh	Readback Count	RO	ZZZZZZ	xxxxx???	??? = Readback count; Cleared when frame sent

APPENDIX B

V233 Register and Memory Descriptions

TABLE OF CONTENTS

VME Access.....	Page 2
On-Board DRAM.....	Page 2
Internal FPGA Control Registers.....	Page 9
Global Registers.....	Page 9
VME ID Registers.....	Page 9
Page Register.....	Page 9
Interrupt Level Register.....	Page 10
Interrupt Vector Register.....	Page 10
Interrupt Enable Register.....	Page 10
Main Interrupt Status Register.....	Page 11
Main Polling Status Register.....	Page 11
System Reset Register.....	Page 12
Channel Arm Register.....	Page 12
Simulated Event Link Code Register.....	Page 12
Event Link Simulator Control Register.....	Page 12
Switch Buffer Ready Register.....	Page 13
User Switch Code Register.....	Page 13
User Code Registers.....	Page 13
User History Register.....	Page 15
A32 Address Map Register.....	Page 16
Channel Registers.....	Page 16
Channel X Interrupt Enable Registers.....	Page 17
Channel X Interrupt Status Registers.....	Page 18
Channel X Polling Status Registers.....	Page 19
Channel X Reset Registers.....	Page 20
Channel X VME Commands Registers.....	Page 21
Channel X Clock Select Registers.....	Page 22
Channel X Missing Readback Count Registers.....	Page 23
Channel X Active Buffers Registers.....	Page 23
Channel X Setpoint Count Registers.....	Page 24
Channel X Frame ID Registers.....	Page 25
Channel X Start Event Registers.....	Page 25
Channel X Resume Event Registers.....	Page 26
Channel X Group End Event Registers.....	Page 28
Channel X Tag Event Registers.....	Page 29
Channel X Switch Active Buffer Registers.....	Page 30
Channel X Start Delay Registers.....	Page 31
Channel X Resume Delay Registers.....	Page 39
Channel X Single Frame Registers.....	Page 71

VME ACCESS

There are two VME addressable areas in the Function Generator module. The first area, consisting of internal FPGA registers dedicated to the module's operational control, is accessed using A24 addressing and D16 or D08(EO) data transfers. An address modifier of 39h or 3Dh must be used for all of these transfers. Address bits A23 -> A14 are used to formulate the module's A24 base address, leaving 16Kbytes of addressable space. Naturally, not every address has a register assigned to it.

The second addressable area consists of on-board DRAM, used for the storage of functions and status Readbacks. This area is accessed using A32 addressing and D32 data transfers. All DRAM data transfers require an address modifier of 09h or 0Dh. Address bits A31-> A22 are used to formulate the module's A32 base address, leaving 4Mbytes of addressable space, called a "Page". In actuality, there is much more on-board DRAM space (512Mbytes, or 128 pages) that needs to be accessed. To accomplish this, a "Page" register is used.

ON-BOARD DRAM

The module's DRAM is used to store Setpoints, which are loaded via the VME interface. The module will then send the Setpoints to a Power Supply Interface (PSI) at a pre-defined rate. Collectively, the Setpoints make up what is known as a "function". The DRAM is also used to store Readback data, retrieved from the PSI after each Setpoint is delivered. There are 6 Readback words for each Setpoint sent. After a function is sent, the Readbacks can be acquired over the VME interface.

Each Setpoint stored in the DRAM is configured into 32 bits. The lower 16 bits are the actual Setpoint, and the upper 16 overhead bits are used to set up function pauses, or to identify the end of the function. Each Readback word is also 32 bits. The lower 24 bits are the PSI information, and the upper 8 bits provide a descriptive overhead. Since a DRAM page is 4Mbytes, and it takes 4 bytes to make up a Setpoint word or a Readback word, each DRAM page actually comprises 1 Meg of words, or 1Mword.

The V233 module has 4 channels of power supply control. Each channel has 32Mwords of the on-board DRAM dedicated to it. In turn, each channel is partitioned as shown below:

User 1 Setpoints, Buffer 1 (1Mword)
User 2 Setpoints, Buffer 1 (1Mword)
User 3 Setpoints, Buffer 1 (1Mword)
User 4 Setpoints, Buffer 1 (1Mword)
User 5 Setpoints, Buffer 1 (1Mword)
User 6 Setpoints, Buffer 1 (1Mword)
User 7 Setpoints, Buffer 1 (1Mword)
User 8 Setpoints, Buffer 1 (1Mword)

User 1 Setpoints, Buffer 2 (1Mword)
User 2 Setpoints, Buffer 2 (1Mword)
User 3 Setpoints, Buffer 2 (1Mword)
User 4 Setpoints, Buffer 2 (1Mword)
User 5 Setpoints, Buffer 2 (1Mword)
User 6 Setpoints, Buffer 2 (1Mword)
User 7 Setpoints, Buffer 2 (1Mword)
User 8 Setpoints, Buffer 2 (1Mword)

Appendix B - V233 Register And Memory Descriptions

Readbacks, Buffer 1 (8Mwords)

Readbacks, Buffer 2 (8Mwords)

As can be seen, each user within a channel has 2 buffers of Setpoints, and 2 buffers of Readbacks. The buffers alternate between active and inactive states. The module's power up default condition is that all "1" buffers are active, but since all channels on the module are disarmed, the "1" buffers are not "fully" active. The initial function (Setpoints) should be written into the "1" buffers, but prior to arming the channels. Once the Setpoints are loaded into the "1" buffers, the channels can be armed. The "1" buffers are then fully active. While an active User Setpoint buffer is being used by the module to send Setpoints to a PSI, the corresponding inactive User Setpoint buffer can be loaded with a new function. An active Setpoint buffer can be read by the VME controller, but it cannot be written. The only exception to this is when the channel is disarmed.

The active Readback buffer is used to store power supply status. Both the active and inactive Readback buffers can be read at any time. They should never be written to with the VME interface, unless for testing purposes.

The Readback buffers change from active to inactive, and visa-versa, upon every occurrence of the Group End event on the Event Link. A User Setpoint buffer will also change from active to inactive, and visa-versa, upon the occurrence of the Group End event, but only if the appropriate bit is set in the Switch Active Buffer Register. This register is described later in this document. It is worth noting that during normal operation different User Setpoint buffers can have their "1" buffers be active, while others have their "2" buffers active.

The bit-map for Setpoint words is shown below in Figure 1. Data bits D15 -> D0 make up the actual Setpoint. Data bits D28 -> D21 Are the Auxiliary bits. Data bits D30 and D29 are unused. Of the 6 overhead bits, D31 and D20 -> D16, only 1 should be set in any single Setpoint word.

Bits D16, D17, D18, D19, or D20, when set, pauses the function. The Setpoint with the set pause bit will be continually sent (repeated) to the PSI until the channel is instructed to resume the function. If D16, D17, D18, or D19 are set, the function will resume only when a predefined Resume event, associated with an active pause bit, occurs on the Event Link. D16 through D19 can each be linked to unique Event Link words. When D20 is set, the function will only resume upon a VME command.

Bit D31 of the Setpoint word defines that Setpoint as the last word of the function. When this Setpoint is sent to the PSI, the module stops reading the DRAM for any more Setpoints. However, the last Setpoint is continually sent (repeated) to the PSI until a Group End event occurs on the Event Link, or until the channel is disarmed.

If more than 1 of the Setpoint overhead bits is inadvertently set, only 1 bit will be recognized. The order of recognition is D31, (the End Function bit), followed by D16, D17, D18, D19, and D20.

Appendix B - V233 Register And Memory Descriptions

The bit-map for Readback words is shown below in Figure 2. Data bits D23 -> D0 make up the actual Readback value retrieved from the PSI. D15 -> D0 are the power supply status bits, and D23 -> D16 are the status ID.

As stated earlier, there are 6 Readback words per Setpoint. The state of the Readback overhead bits, with the exception of the CRC Error bit, will be the same for all 6 words. The Readback overhead bits are defined as follows:

D31: Start Function...If set, D31 indicates that the Readback word is associated with the first Setpoint of a function. The first 6 Readbacks at the top of the Readback buffer should always have this bit set. The only time any other words in the Readback buffer could have this bit set is if another Start event occurs prior to the Group End event.

D30: Pause Function...Bit D30 is set in every Readback word acquired while the function is paused. It is possible for D31 and D30 to be set at the same time, but only if the first Setpoint of the function has a pause bit set.

D29: End Function...Bit D29 is set in every Readback word acquired after the last Setpoint of the function is sent. Remember, the last Setpoint is repeated until the Group End event occurs.

It is possible for D31 and D30 to be set at the same time if the first Setpoint of a function has a pause bit set. It is also possible for D31 and D29 to be set at the same time, but only if a function has a single Setpoint. Bits D30 and D29 should never be set in the same Readback word.

D28 -> D26: User Code...000 = User 1, 001 = User 2, 010 = User 3, 011 = User 4, 100 = User 5, 101 = User 6, 110 = User 7, and 111 = User 8.

D25: End of Table (EOT)...When D25 is set, all the other bits are set to zero. D25 is only set in one case. Upon a Group End event, Setpoint transmissions are halted, and no more Readbacks are taken. The value 02000000h is loaded into the Readback buffer immediately following the last stored Readback. This is done to mark the end of the Readbacks associated with the previous function that was sent. It should be noted that when the Group End event occurs, all acquisition of Readbacks is halted immediately. Therefore, it is possible that the last Setpoint sent will not have its full complement of 6 Readback words saved in the Readback buffer. In fact, depending on the timing, the last Setpoint could have anywhere from zero Readbacks to as many as all 6 Readbacks.

If the Readback buffer overflows prior to the Group End event, no EOT word will be stored in the buffer.

D24: CRC Error...If set, Readback word was retrieved with a CRC error.

Appendix B - V233 Register And Memory Descriptions

Prior to any VME data transfers to or from the DRAM, the Page register must be set-up in order to access the appropriate section of memory, or “page”. The Page Register’s main function is to provide the upper address bits needed to access a particular 1Mword page of DRAM. However, it can also be used during a VME transfer to access either an active or inactive buffer, without actually knowing which buffer is active and which buffer is inactive.

The Page Register is 16 bits, but only the lower 9 bits, D8 -> D0, are used. The upper 7 bits are “don’t cares”. The bit-map is shown below in Figure 3.

Page Register Bit-Map

D8	D7	ADDRESS MODE	D6	D5	DRAM	D4	D3	D2	D1	D0	PAGE (4Mbytes, 1Mword)
0	X	Any Buffer	0	0	Chan 1	0	0	0	0	0	Buffer 1, User 1 Setpoints
1	0	Inactive Buffer (D4 = X)	0	1	Chan 2	0	0	0	0	1	Buffer 1, User 2 Setpoints
1	1	Active Buffer (D4 = X)	1	0	Chan 3	0	0	0	1	0	Buffer 1, User 3 Setpoints
			1	1	Chan 4	0	0	0	1	1	Buffer 1, User 4 Setpoints
						0	0	1	0	0	Buffer 1, User 5 Setpoints
						0	0	1	0	1	Buffer 1, User 6 Setpoints
						0	0	1	1	0	Buffer 1, User 7 Setpoints
						0	0	1	1	1	Buffer 1, User 8 Setpoints
						0	1	0	0	0	Buffer 1, Page 1 Readback
						0	1	0	0	1	Buffer 1, Page 2 Readback
						0	1	0	1	0	Buffer 1, Page 3 Readback
						0	1	0	1	1	Buffer 1, Page 4 Readback
						0	1	1	0	0	Buffer 1, Page 5 Readback
						0	1	1	0	1	Buffer 1, Page 6 Readback
						0	1	1	1	0	Buffer 1, Page 7 Readback
						0	1	1	1	1	Buffer 1, Page 8 Readback
						1	0	0	0	0	Buffer 2, User 1 Setpoints
						1	0	0	0	1	Buffer 2, User 2 Setpoints
						1	0	0	1	0	Buffer 2, User 3 Setpoints
						1	0	0	1	1	Buffer 2, User 4 Setpoints
						1	0	1	0	0	Buffer 2, User 5 Setpoints
						1	0	1	0	1	Buffer 2, User 6 Setpoints
						1	0	1	1	0	Buffer 2, User 7 Setpoints
						1	0	1	1	1	Buffer 2, User 8 Setpoints
						1	1	0	0	0	Buffer 2, Page 1 Readback
						1	1	0	0	1	Buffer 2, Page 2 Readback
						1	1	0	1	0	Buffer 2, Page 3 Readback
						1	1	0	1	1	Buffer 2, Page 4 Readback
						1	1	1	0	0	Buffer 2, Page 5 Readback
						1	1	1	0	1	Buffer 2, Page 6 Readback
						1	1	1	1	0	Buffer 2, Page 7 Readback
						1	1	1	1	1	Buffer 2, Page 8 Readback

When D8 = 1, D7 determines whether the active or inactive buffers are accessed. D4 becomes "don't care"

Figure 3

Appendix B - V233 Register And Memory Descriptions

It should be noted that a User Setpoint buffer, active or inactive, is exactly 1 page in size. This means the Page Register only needs to be set-up once prior to accessing a User Setpoint buffer. However, a Readback buffer spans 8 pages. This means that if all 8Mwords of a Readback buffer needed to be read, the Page Register would have to be set-up 8 times during the read process...Once prior to reading the 1st page, then again prior to reading the 2nd page, and so on, until all 8 pages have been read.

Bits D6 and D5 combine to determine which channel's buffers are being accessed.

When D8 of the Page Register is zero, the VME transfer can be for any active or inactive buffer. In this case, D7 is a "don't care" bit. However, when D8 is set, D7 determines whether the access is for an active or inactive buffer. If D8 is set and D7 is zero, the access is for an inactive buffer. If D8 is set and D7 is set, the access is for an active buffer. Setting D8 essentially makes D4 a "don't care" bit, because D4 normally determines whether a "1" buffer or a "2" buffer is being accessed.

Remember! An active Setpoint buffer cannot be written using the VME interface. The V233 will provide a *DTACK signal, making it appear that the write was successful, but unless the channel is dis-armed, no VME writes to an active Setpoint buffer will be successfully executed.

INTERNAL FPGA CONTROL REGISTERS

Internal FPGA registers are used to configure, operate, and obtain status for the V233. Some registers are global in nature, affecting the operation of the board across all channels. Other registers are applied on a channel-by-channel basis. All registers are accessed through normal A24/D16 or A24/D08(EO) VME transfers. In the case of 16-bit registers, data bits D7 -> D0 comprise the low byte, and D15 -> D8 comprise the high byte. Unless stated otherwise, the power-up state for all register bits is zero.

GLOBAL REGISTERS

The following descriptions are for the board's global registers. The VME addresses shown next to each register are to be applied as offsets to the A24 base address.

VME ID Registers (Read Only, 1 byte/character) VME addresses H0000 -> H001F

These registers provide an ASCII identity string for the V233 module, which includes the board's ID number (V233), revision letter, and a 4-digit serial number. The string is shown below. ASCII characters are enclosed in quotation marks, which are not actually included in the string. Hexadecimal zeros are used as string separators.

“VMEIDBNLV233”0000h”REVx”0000h”SER#xxxx”00000000h.

Page Register (Read/Write, 2 bytes) VME addresses H0020 -> H0021

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don't Care”
 D8 0 = access any buffer, 1 = access active or inactive buffer
 D7 If D8 = 0, D7 = “don't care”.
 If D8 = 1, D7 =0, access inactive buffer
 If D8 = 1, D7 =1, access active buffer
 D6 -> D5 00 = channel 1, 01 = channel 2, 10 = channel 3, 11 = channel 4
 D4 0 = buffer 1, 1 = buffer 2
 D3 -> D0 Determines individual page.

*See Figure 3 for page mapping description

Appendix B - V233 Register And Memory Descriptions

Interrupt Level Register (Read/Write, 1 byte)

VME address H0023

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	1/0	1/0	1/0

D7 -> D3 “Don’t Care”

D2 -> D0 Determines Interrupt level

000 = Interrupt Disabled, 001 = IRQ1*, 010 = IRQ2*, 011 = IRQ3*,
100 = IRQ4*, 101 = IRQ5*, 110 = IRQ6*, 111 = IRQ7*

Interrupt Vector Register (Read/Write, 2 bytes)

VME address H0024 -> H0025

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Determines 16 bit STATUS/ID (vector)

Interrupt Enable Register (Read/Write, 1 byte)

VME address H0027

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	X	1/0	1/0	1/0

D7 1 = enable Channel 4 interrupts, 0 = disable Channel 4 interrupts

D6 1 = enable Channel 3 interrupts, 0 = disable Channel 3 interrupts

D5 1 = enable Channel 2 interrupts, 0 = disable Channel 2 interrupts

D4 1 = enable Channel 1 interrupts, 0 = disable Channel 1 interrupts

D3 “Don’t Care”

D2 1 = enable Event Link parity error interrupt, 0 = disable

D1 1 = enable Event Link “carrier up” interrupt, 0 = disable

D0 0 = enable Event Link “carrier down” interrupt, 0 = disable

* a carrier up interrupt will not occur unless carrier was previously in a down state

** a carrier down interrupt will not occur unless carrier was previously in an up state

*** individual channel interrupts are set in separate registers

Appendix B - V233 Register And Memory Descriptions

Main Interrupt Status Register (Read Only/Auto Clear, 2 bytes) VME address H0028

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

- D15 -> D12 Always zero
- D11 1 = Board Ready (following power-up or reset)
- D10 -> D8 Active User (000 = User 1, 001 = User 2,... 111 = User 8)
- D7 1 = Channel 4 interrupt condition, 0 = no interrupt condition
- D6 1 = Channel 3 interrupt condition, 0 = no interrupt condition
- D5 1 = Channel 2 interrupt condition, 0 = no interrupt condition
- D4 1 = Channel 1 interrupt condition, 0 = no interrupt condition
- D3 1 = Valid Event Link word occurred
- D2 1 = Event Link word with parity error occurred
- D1 1 = Event Link carrier up (from carrier down state)
- D0 1 = Event Link carrier down (from carrier up state)

Once any of the lower 8 bits are set in the Main Interrupt Status register, they remains set until read by the VME controller. Reading the register clears the lower 8 bits.

Use the Main Interrupt Status register for checking the status of the module during an interrupt routine. Because of potential conflicts between the occurrence of an interrupt and routine polling of the board's status, this register should not be used for polling.

Main Polling Status Register (Read Only/Auto Clear, 2 bytes) VME address H002A

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

- D15 -> D12 Always zero
- D11 1 = Board Ready (following power-up or reset)
- D10 -> D8 Active User (000 = User 1, 001 = User 2,... 111 = User 8)
- D7 1 = Channel 4 interrupt condition, 0 = no interrupt condition
- D6 1 = Channel 3 interrupt condition, 0 = no interrupt condition
- D5 1 = Channel 2 interrupt condition, 0 = no interrupt condition
- D4 1 = Channel 1 interrupt condition, 0 = no interrupt condition
- D3 1 = Valid Event Link word occurred
- D2 1 = Event Link word with parity error occurred
- D1 1 = Event Link carrier up (from carrier down state)
- D0 1 = Event Link carrier down (from carrier up state)

Once any of the lower 8 bits are set in the Main Polling Status register, they remain set until read by the VME controller. Reading the register clears the lower 8 bits.

Use the Main Polling Status Register for regular polling of the module's status. Because of potential conflicts between polling and the occurrence of an interrupt, this register should not be used for checking interrupt status.

Appendix B - V233 Register And Memory Descriptions

System Reset Register (Write Only/Auto Clear, 1 byte)

VME address H002D

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	Z	Z	Z	1/0

D7 -> D1 “No Access”
 D0 1 = reset module, 0 = no affect

Resetting the Function Generator module will put all registers into their default state, and all channels will be disarmed. This will halt any ongoing functions. Care should be taken when doing this during an active function, because the power supply will be left at the state determined by the last Setpoint sent.

Channel Arm Register (Read/Write, 1 byte)

VME address H002F

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	1/0	1/0	1/0	1/0

D7 -> D4 “Don’t Care”
 D3 1 = arm Channel 4, 0 = disarm Channel 4
 D2 1 = arm Channel 3, 0 = disarm Channel 3
 D1 1 = arm Channel 2, 0 = disarm Channel 2
 D0 1 = arm Channel 1, 0 = disarm Channel 1

*Arming a channel should always be the last step when configuring the Function Generator module.

Simulated Event Link Code Register (Read/Write, 1 byte)

VME address H0031

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 Event Link word used to synchronize switching of setpoint buffers

Event Link Simulator Control Register (Read/Write, 1 byte)

VME address H0033

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	1/0	1/0

D7 -> D2 “Don’t Care”
 D1 1 = send simulated Event (bit auto clears after transmission)
 D0 1 = simulator mode on, 0 = simulator mode off

Appendix B - V233 Register And Memory Descriptions

Switch Buffer Ready Register (Read/Write, 2 bytes) VME address H0034 -> H0035

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable setpoint buffer switching synchronization, 0 = disable

D7 -> D0 Event Link word used to “pre-switch” setpoint buffers

User Switch Code Register (Read/Write, 2 bytes) VME address H0040 -> H0041

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable PPM, 0 = disable PPM

D7 -> D0 Event Link word used to switch users

* User 1 is the active user at power up.

** If PPM is disabled, the User 1 registers are used to configure and operate the module.

*** It is permissible to use the same Event Link word defined as the User Switch Code to start a function.

User 1 Code Register (Read/Write, 2 bytes) VME address H0042 -> H0043

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 1, 0 = disable User 1

D7 -> D0 Event Link word used to prepare to switch to User 1

*If a user is disabled, the last active user will remain active

User 2 Code Register (Read/Write, 2 bytes) VME address H0044 -> H0045

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 2, 0 = disable User 2

D7 -> D0 Event Link word used to prepare to switch to User 2

* If a user is disabled, the last active user will remain active

Appendix B - V233 Register And Memory Descriptions

User 3 Code Register (Read/Write, 2 bytes)

VME address H0046 -> H0047

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 3, 0 = disable User 3

D7 -> D0 Event Link word used to prepare to switch to User 3

*If a user is disabled, the last active user will remain active

User 4 Code Register (Read/Write, 2 bytes)

VME address H0048 -> H0049

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 4, 0 = disable User 4

D7 -> D0 Event Link word used to prepare to switch to User 4

*If a user is disabled, the last active user will remain active

User 5 Code Register (Read/Write, 2 bytes)

VME address H004A -> H004B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 5, 0 = disable User 5

D7 -> D0 Event Link word used to prepare to switch to User 5

*If a user is disabled, the last active user will remain active

User 6 Code Register (Read/Write, 2 bytes)

VME address H004C -> H004D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 6, 0 = disable User 6

D7 -> D0 Event Link word used to prepare to switch to User 6

* If a user is disabled, the last active user will remain active

Appendix B - V233 Register And Memory Descriptions

User 7 Code Register (Read/Write, 2 bytes)

VME address H004E -> H004F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 7, 0 = disable User 7

D7 -> D0 Event Link word used to prepare to switch to User 7

*If a user is disabled, the last active user will remain active

User 8 Code Register (Read/Write, 2 bytes)

VME address H0050 -> H0051

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = enable User 8, 0 = disable User 8

D7 -> D0 Event Link word used to prepare to switch to User 8

*If a user is disabled, the last active user will remain active

User History Register (Read Only/Write To Clear, 1 byte)

VME address H0053

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 1 = User 8 was active, 0 = User 8 was not active

D6 1 = User 7 was active, 0 = User 7 was not active

D5 1 = User 6 was active, 0 = User 6 was not active

D4 1 = User 5 was active, 0 = User 5 was not active

D3 1 = User 4 was active, 0 = User 4 was not active

D2 1 = User 3 was active, 0 = User 3 was not active

D1 1 = User 2 was active, 0 = User 2 was not active

D0 1 = User 1 was active, 0 = User 1 was not active

This register allows the operator to see what users have been active. To clear an active user indication, write a “1” to the applicable bit location, which clears the bit. Multiple bits can be cleared simultaneously. Writing a “0” to a bit location will have no effect on the state of the bit.

Appendix B - V233 Register And Memory Descriptions

A32 Address Map Register (Read Only, 2 bytes)

VME address H0060 -> H061

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
0	0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D10 Always zero

D9 -> D0 Represents the 10 position switch setting (A31 -> A22) that determines the module's A32 base address.

CHANNEL REGISTERS

The following descriptions are for individual channel registers. The VME addresses shown next to each register are to be applied as offsets to the A24 base address.

Appendix B - V233 Register And Memory Descriptions

Channel X Interrupt Enable Register (Read/Write, 2 bytes)

Channel 1 Interrupt Enable Register: VME address H0800 -> H0801

Channel 2 Interrupt Enable Register: VME address H1000 -> H1001

Channel 3 Interrupt Enable Register: VME address H1800 -> H1801

Channel 4 Interrupt Enable Register: VME address H2000 -> H2001

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	X	X	1/0	1/0	1/0

- D15 1 = enable Run interrupt, 0 = disable interrupt. The Run interrupt occurs when a new function starts. The next Run interrupt cannot occur unless preceded by a Group End Event or a User Change Event.
- D14 1 = enable End Function interrupt, 0 = disable interrupt. The End Function interrupt occurs when the last Setpoint of a function is sent. The next End Function interrupt cannot occur unless preceded by a Group End Event.
- D13 1 = enable Group End interrupt, 0 = disable interrupt. The Group End interrupt occurs when a Group End Event occurs .
- D12 1 = enable End Of Function Error interrupt, 0 = disable interrupt. The End Of Function Error interrupt occurs when a User Change Event or a Group End Event occurs a function has completed.
- D11 1 = enable Pause 4 interrupt, 0 = disable interrupt.
- D10 1 = enable Pause 3 interrupt, 0 = disable interrupt.
- D9 1 = enable Pause 2 interrupt, 0 = disable interrupt.
- D8 1 = enable Pause 1 interrupt, 0 = disable interrupt.
- D7 1 = enable VME Pause interrupt, 0 = disable interrupt.
All Pause interrupts occur at the start of a pause. The next Pause interrupt cannot occur unless the function is first resumed.
- D6 1 = enable Readback Overflow interrupt, 0 = disable interrupt. The Readback Overflow interrupt occurs when more than 8Mwords of Readbacks have been received between the start of a function and a Group End Event.
- D5 1 = enable Setpoint Overflow interrupt, 0 = disable interrupt. The Setpoint Overflow interrupt occurs when no End-Of-Function bit was seen before reaching the end of the Setpoint buffer.
- D4 “Don’t Care”
- D3 “Don’t Care”
- D2 1 = enable PSI Input Link CRC Error interrupt, 0 = disable interrupt. A PSI Input Link CRC Error interrupt occurs when a CRC error was detected during the reception of a Readback word.
- D1 1 = enable PSI Input Link Up interrupt, 0 = disable interrupt. A PSI Input Link Up interrupt won’t occur unless the link was previously down.
- D0 1 = enable PSI Input Link Down interrupt, 0 = disable interrupt. A PSI Input Link Down interrupt won’t occur unless the link was previously up.

Appendix B - V233 Register And Memory Descriptions

Channel X Interrupt Status Register (Read Only/Auto Clear, 2 bytes)

Channel 1 Interrupt Status Register: VME address H0802 -> H0803

Channel 2 Interrupt Status Register: VME address H1002 -> H1003

Channel 3 Interrupt Status Register: VME address H1802 -> H1803

Channel 4 Interrupt Status Register: VME address H2002 -> H2003

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

- D15 1 = Setpoints being sent. (Including pauses and after the end of function, until the Group End Event occurs) Cleared by Group End Event.
- D14 1 = end of function occurred, but the Group End Event has not. (The last Setpoint value is being repeated) Cleared by Group End Event.
- D13 1 = Group End Event occurred.
- D12 1 = End Of Function Error occurred. (User Change Event or Group End Event seen before the end of function)
- D11 1 = Pause 4 active.
- D10 1 = Pause 3 active.
- D9 1 = Pause 2 active.
- D8 1 = Pause 1 active.
- D7 1 = VME Pause active.
- D6 1 = Readback Overflow occurred. A Readback Overflow occurs when more than 8Mwords of Readbacks have been received between the start of a function and a Group End Event.
- D5 1 = Setpoint Overflow occurred. A Setpoint Overflow occurs when no End-Of-Function bit was seen before reaching the end of a Setpoint buffer.
- D4 1 = No Readback seen from PSI between any two sent Setpoints.
- D3 1 = word received on PS Input Link.
- D2 1 = PS Input Link CRC Error occurred.
- D1 1 = PS Input Link Up
- D0 1 = PS Input Link Down

Once a bit is set in a Channel Interrupt Status register, it remains set until the register is read by the VME controller. Reading the register clears all the bits. However, if any inputs are still active, their bits will immediately be reset.

Use a Channel Interrupt Status register for checking the status of a module's channel during an interrupt routine. Because of potential conflicts between the occurrence of an interrupt and routine polling of a channel's status, this register should not be used for polling.

Appendix B - V233 Register And Memory Descriptions

Channel X Polling Status Register (Read Only/Auto Clear, 2 bytes)

Channel 1 Polling Status Register: VME address H0804 -> H0805

Channel 2 Polling Status Register: VME address H1004 -> H1005

Channel 3 Polling Status Register: VME address H1804 -> H1805

Channel 4 Polling Status Register: VME address H2004 -> H2005

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

- D15 1 = Setpoints being sent. (Including pauses and after the end of function, until the Group End Event occurs) Cleared by Group End Event.
- D14 1 = end of function occurred, but the Group End Event has not. (The last Setpoint value is being repeated) Cleared by Group End Event.
- D13 1 = Group End Event occurred.
- D12 1 = End Of Function Error occurred. (User Change Event or Group End Event seen before the end of function)
- D11 1 = Pause 4 active.
- D10 1 = Pause 3 active.
- D9 1 = Pause 2 active.
- D8 1 = Pause 1 active.
- D7 1 = VME Pause active.
- D6 1 = Readback Overflow occurred. A Readback Overflow occurs when more than 8Mwords of Readbacks have been received between the start of a function and a Group End Event.
- D5 1 = Setpoint Overflow occurred. A Setpoint Overflow occurs when no End-Of-Function bit was seen before reaching the end of a Setpoint buffer.
- D4 1 = No Readback seen from PSI between any two sent Setpoints.
- D3 1 = word received on PS Input Link.
- D2 1 = PS Input Link CRC Error occurred.
- D1 1 = PS Input Link Up
- D0 1 = PS Input Link Down

Once a bit is set in a Channel Polling Status register, it remains set until the register is read by the VME controller. Reading the register clears all the bits. However, if any inputs are still active, their bits will immediately be reset.

Use a Channel Polling Status register for regular polling of the channel's status. Because of potential conflicts between the occurrence of an interrupt and routine polling of a channel's status, this register should not be used for checking interrupt status.

Appendix B - V233 Register And Memory Descriptions

Channel X Reset Register (Write Only/Auto Clear, 1 byte)

Channel 1 Reset Register: VME address H0807

Channel 2 Reset Register: VME address H1007

Channel 3 Reset Register: VME address H1807

Channel 4 Reset Register: VME address H2007

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	Z	Z	Z	1/0

D7 -> D1 "No Access"

D0 1 = reset module, 0 = no affect

Resetting a channel will put all the channel specific registers into their default state, and the channel will be disarmed. This will halt any ongoing function. Care should be taken when doing this during an active function, because the power supply will be left at the state determined by the last Setpoint sent.

After the reset has been accomplished, the register is automatically cleared.

Channel X VME Commands Register (Write Only/Auto Clear, 1 byte)

Channel 1 Start And Resume Register: VME address H0809

Channel 2 Start And Resume Register: VME address H1009

Channel 3 Start And Resume Register: VME address H1809

Channel 4 Start And Resume Register: VME address H2009

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	1/0	1/0	1/0	1/0

D7 -> D4 “No Access”

D3 1 = send Tag command, 0 = no affect

D2 1 = send Group End command, 0 = no affect

D1 1 = send Resume command, (from a VME Pause state), 0 = no affect

D0 1 = send Start command, 0 = no affect

Using D0 of this register will cause the channel to simulate a Start event, allowing the operator to start a function with a VME command, instead of using an event on the Event Link. Remember, the channel must be armed prior to starting a function. There is no programmable delay for a VME Start command, but there will be a built-in 10us delay, allowing time for the PSI to finish responding to any previously transmitted Setpoint.

If the channel is in a VME Pause, as determined by the overhead bit D20 of a Setpoint, writing a “1” to D1 of the Channel X VME Command register will cause the function to resume. There is no programmable delay for a VME Resume command, but there will be a built-in 10us delay, allowing time for the PSI to finish responding to any previously transmitted Setpoint.

Setting D2 of this register will cause the channel to simulate a Group End event, ending the transmission of any setpoints, and switching the active and inactive Readback and Setpoint buffers.

Setting D1 of this register will cause the next group of readbacks to be “tagged”.

If an attempt is made to set more than 1 bit simultaneously in the VME Commands register, only 1 bit will be recognized. The order of priority is D0, D1, D2, and then D3. The register is automatically cleared immediately after any bit is set.

The VME Start bit and Group End bits should be used carefully. Once a channel is armed, any start instruction, initiated through VME or the Event Link, will begin a function. Any start instructions that occur during an active function will re-start the function. This may cause an abrupt and large change at the output of the power supply. Applying a Group End bit prematurely may leave a power supply in an undesirable state.

Channel X Clock Select Register (Read/Write, 1 byte)

Channel 1 Clock Select Register: VME address H080B

Channel 2 Clock Select Register: VME address H100B

Channel 3 Clock Select Register: VME address H180B

Channel 4 Clock Select Register: VME address H200B

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

- D7 1 = enable External “Group End” pulse, 0 = disable
- D6 1 = enable External “Resume” pulse, 0 = disable
- D5 1 = enable External “Start” pulse, 0 = disable
- D4 1 = clocks derived internally, 0 = clocks derived from Event Link
- D3 1 = Setpoint clock derived from Gauss clock
0 = Setpoint clock determined by D2 -> D0
- D2 -> D0 000 = 10KHz, 001 = 1KHz, 010 = 100Hz, 011 = 100KHz
1XX = 1MHz

There are 4 external inputs available on the Function Generator module: “Group End”, “Resume”, “Start”, and “Gauss Clock”. They all use on-board opto-isolated couplers. The external inputs can be use to perform the same tasks as their Event Link namesakes. (The external “Resume” input is equivalent to a Resume 1 Event.) These inputs are actually “ORed” with their corresponding Event Link inputs, so if the board is to be operated solely with the external inputs, the events should be disabled within the appropriate registers, or the Event Link should be disconnected and D4 should be set. A combination of one, two, or all three external inputs can be used, using Event Link events to perform the other tasks. For instance, an external “Start” pulse can be used to start a function, but a Group End event can be used to end Setpoint transmission.

* The external Resume input doubles as the external Tag input. If the external Tag function is enabled, the external Resume function is automatically disabled.

The “Gauss Clock” input frequency is divided by 100, and the resultant clock can be selected as the Setpoint clock. The maximum Gauss clock frequency is 10MHz. If not using the external “Gauss Clock” input, the Setpoint clock can be programmed to any of the following 5 choices: 10KHz, 1KHz, 100Hz, 100KHz, or 1MHz. The 1MHz clock does not allow the PSI enough time to respond with any readbacks. This setting is not intended for normal operation.

Normally, all internal clocks, including the Setpoint clock, are derived from the Event Link. This provides for repeatable synchronization with events. However, it is possible to operate the board without an Event Link, using VME commands or external inputs to start and resume functions. In this case, all clocks must be derived from an on-board crystal oscillator. Setting D4 to 1 causes the channel to use the on-board oscillator.

Appendix B - V233 Register And Memory Descriptions

Channel X Missing Readback Count Register (Read Only/Auto Clear, 1 byte)

Channel 1 Missing Readback Count Register: VME address H080D

Channel 2 Missing Readback Count Register: VME address H100D

Channel 3 Missing Readback Count Register: VME address H180D

Channel 4 Missing Readback Count Register: VME address H200D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 8 bits of 8-bit Missing Readback counter. D7 is MSB.

The Channel X Missing Readback Count register holds a running count of the number of times no PSI readbacks were seen between any two consecutive setpoints. The count is cleared when read. If the counter reaches its maximum value of 255, it freezes there until cleared by a read.

Channel X Active Buffers Register (Read Only, 2 bytes)

Channel 1 Active Buffers Register: VME address H080E -> H080F

Channel 2 Active Buffers Register: VME address H100E -> H100F

Channel 3 Active Buffers Register: VME address H180E -> H180F

Channel 4 Active Buffers Register: VME address H200E -> H200F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Readback Buffer “2” active, 0 = Readback Buffer “1” active

D7 1 = User 8 Setpoint buffer “2” active, 0 = buffer “1” active

D6 1 = User 7 Setpoint buffer “2” active, 0 = buffer “1” active

D5 1 = User 6 Setpoint buffer “2” active, 0 = buffer “1” active

D4 1 = User 5 Setpoint buffer “2” active, 0 = buffer “1” active

D3 1 = User 4 Setpoint buffer “2” active, 0 = buffer “1” active

D2 1 = User 3 Setpoint buffer “2” active, 0 = buffer “1” active

D1 1 = User 2 Setpoint buffer “2” active, 0 = buffer “1” active

D0 1 = User 1 Setpoint buffer “2” active, 0 = buffer “1” active

The Channel X Active Buffers register is a status register, allowing the operator to see which Setpoint and Readback buffers are presently active.

Appendix B - V233 Register And Memory Descriptions

Channel X Setpoint Count High Register (Read Only, 1 byte)

Channel 1 Setpoint Count High Register: VME address H0811

Channel 2 Setpoint Count High Register: VME address H1011

Channel 3 Setpoint Count High Register: VME address H1811

Channel 4 Setpoint Count High Register: VME address H2011

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit Setpoint counter

Channel X Setpoint Count Low Register (Read Only, 2 bytes)

Channel 1 Setpoint Count Low Register: VME address H0812 -> H0813

Channel 2 Setpoint Count Low Register: VME address H1012 -> H1013

Channel 3 Setpoint Count Low Register: VME address H1812 -> H1813

Channel 4 Setpoint Count Low Register: VME address H2012 -> H2013

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit Setpoint counter

The Channel X Setpoint High Count register and Channel X Setpoint Low Count register combine to provide the latched output of a 24-bit Setpoint counter. The counter keeps track of the number of Setpoints actually transmitted to a PSI between Group End events, including those sent during pauses, and during the period from the end of a function to the occurrence of a Group End event. The counter's output is latched on Group End, and then the counter is reset. The Setpoint Count registers do not provide a running count of Setpoints. They are only updated on the occurrence of the Group End event.

Appendix B - V233 Register And Memory Descriptions

Channel X Frame ID Register (Read/Write, 1 byte)

Channel 1 Frame ID Register: VME address H0815

Channel 2 Frame ID Register: VME address H1015

Channel 3 Frame ID Register: VME address H1815

Channel 4 Frame ID Register: VME address H2015

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 PSI Frame ID

The Channel X Frame ID register determines the Frame ID that is used when formatting a setpoint into the 43-bit word sent to the PSI.

Channel X Start Event Register (Read/Write, 2 bytes)

Channel 1 Start Event Register: VME address H0820 -> H0821

Channel 2 Start Event Register: VME address H1020 -> H1021

Channel 3 Start Event Register: VME address H1820 -> H1821

Channel 4 Start Event Register: VME address H2020 -> H2021

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Start event register active, 0 = Start event register inactive

D7 -> D0 Defines Start event used to initiate the start of a function

This register defines the 8-bit Event Link word that will be used as a channel’s Start event. D8 must be set in order for the module to decode the starting event. If D8 is cleared, no Event Link word will start a function.

Appendix B - V233 Register And Memory Descriptions

Channel X Resume 1 Event Register (Read/Write, 2 bytes)

Channel 1 Resume 1 Event Register: VME address H0822 -> H0823

Channel 2 Resume 1 Event Register: VME address H1022 -> H1023

Channel 3 Resume 1 Event Register: VME address H1822 -> H1823

Channel 4 Resume 1 Event Register: VME address H2022 -> H2023

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Resume 1 event register active, 0 = Resume 1 event register inactive

D7 -> D0 Defines Resume 1 event. Used to resume a function that was paused when overhead bit D16 of a Setpoint word was set

This register defines the 8-bit Event Link word that will be used as a channel’s Resume 1 event. D8 must be set in order for the module to decode the resuming event. If D8 is cleared, no Event Link word can re-start a function that is in a Pause 1 mode.

Channel X Resume 2 Event Register (Read/Write, 2 bytes)

Channel 1 Resume 2 Event Register: VME address H0824 -> H0825

Channel 2 Resume 2 Event Register: VME address H1024 -> H1025

Channel 3 Resume 2 Event Register: VME address H1824 -> H1825

Channel 4 Resume 2 Event Register: VME address H2024 -> H2025

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Resume 2 event register active, 0 = Resume 2 event register inactive

D7 -> D0 Defines Resume 2 event. Used to resume a function that was paused when overhead bit D17 of a Setpoint word was set

This register defines the 8-bit Event Link word that will be used as a channel’s Resume 2 event. D8 must be set in order for the module to decode the resuming event. If D8 is cleared, no Event Link word can re-start a function that is in a Pause 2 mode.

Channel X Resume 3 Event Register (Read/Write, 2 bytes)

Channel 1 Resume 3 Event Register: VME address H0826 -> H0827

Channel 2 Resume 3 Event Register: VME address H1026 -> H1027

Channel 3 Resume 3 Event Register: VME address H1826 -> H1827

Channel 4 Resume 3 Event Register: VME address H2026 -> H2027

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Resume 3 event register active, 0 = Resume 3 event register inactive

D7 -> D0 Defines Resume 3 event. Used to resume a function that was paused when overhead bit D18 of a Setpoint word was set

This register defines the 8-bit Event Link word that will be used as a channel’s Resume 3 event. D8 must be set in order for the module to decode the resuming event. If D8 is cleared, no Event Link word can re-start a function that is in a Pause 3 mode.

Channel X Resume 4 Event Register (Read/Write, 2 bytes)

Channel 1 Resume 4 Event Register: VME address H0828 -> H0829

Channel 2 Resume 4 Event Register: VME address H1028 -> H1029

Channel 3 Resume 4 Event Register: VME address H1828 -> H1829

Channel 4 Resume 4 Event Register: VME address H2028 -> H2029

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 “Don’t Care”

D8 1 = Resume 4 event register active, 0 = Resume 4 event register inactive

D7 -> D0 Defines Resume 4 event. Used to resume a function that was paused when overhead bit D19 of a Setpoint word was set

This register defines the 8-bit Event Link word that will be used as a channel’s Resume 4 event. D8 must be set in order for the module to decode the resuming event. If D8 is cleared, no Event Link word can re-start a function that is in a Pause 4 mode.

Channel X Group End Event Register (Read/Write, 2 bytes)

Channel 1 Group End Event Register: VME address H082A -> H082B

Channel 2 Group End Event Register: VME address H102A -> H102B

Channel 3 Group End Event Register: VME address H182A -> H182B

Channel 4 Group End Event Register: VME address H202A -> H202B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D14 “Don’t Care”

D13 -> D11 Indicates user in which channel must be halted (after function sent)

D10 If set, indicates that the channel has been halted

D9 If set, indicates that the channel must halt after 1st function of user is sent

D8 1 = Group End event register active, 0 = Group End event register inactive

D7 -> D0 Defines Group End event. The Group End event is used to end the transmission of Setpoints, and to switch active buffers.

This register defines the 8-bit Event Link word that will be used as a channel’s Group End event. D8 must be set in order for the module to actually decode the event.

This register can also be used to command a channel to halt after the first function in a particular user is sent, essentially shutting off the channel. When D9 is set, the next Group End event arms the halt utility. Any functions programmed for users appearing before the selected user will be sent in the normal manner. However, after the first function in the selected user is sent, the last setpoint of that function is repeated until another Group End event occurs, regardless of subsequent Start events or user changes. Upon the next Group End event the channel will be halted. If a function does not start in the selected user, the channel will not be put into a halted state. Once a channel is halted, bit D10 is set. A halted channel cannot be re-started until D10 is cleared and another Group End event occurs. D10 cannot be cleared until the Group End event occurs that halts the channel. However, if D10 is cleared before the first function starts in the selected user, the halt utility will be disabled. If D9 remains set after clearing D10, and a function in the selected user is started, the channel will halt again upon the occurrence of a Group End event.

Appendix B - V233 Register And Memory Descriptions

Channel X Tag Event Register (Read/Write, 2 bytes)

Channel 1 Tag Event Register: VME address H082C -> H082D

Channel 2 Tag Event Register: VME address H102C -> H102D

Channel 3 Tag Event Register: VME address H182C -> H182D

Channel 4 Tag Event Register: VME address H202C -> H202D

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	X	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D10 "Don't Care"

D9 If set, indicates external tag input is active

D8 1 = Tag Event register active, 0 = Tag Event register inactive

D7 -> D0 Defines Tag event. The Tag event is used to set the tag bit in a set of readbacks from the PSI.

Readbacks are tagged in order to help identify specific readbacks in a large buffer with a precise point in time.

The Tag Event register defines the 8-bit Event Link word that will be used as a channel's Tag event. D8 must be set in order for the module to actually decode the event. Once the Tag event is received, the tag is active from the first setpoint sent after the Tag event occurs to the following setpoint. If six readbacks are received following the first setpoint, each one will have its tag bit set.

The V233's External Resume input doubles as the Tag input. Setting D9 of a channel's Tag Event register uses the external input as a tag input. Other channels can still use the input as an external Resume input, but such a setup could prove confusing to the operator if used in this manner.

Channel X Switch Active Buffer Registers (Write Only/Auto Clear, 1 byte)

Channel 1 User 1 Switch Active Buffer Register: VME address H0831
 Channel 1 User 2 Switch Active Buffer Register: VME address H0833
 Channel 1 User 3 Switch Active Buffer Register: VME address H0835
 Channel 1 User 4 Switch Active Buffer Register: VME address H0837
 Channel 1 User 5 Switch Active Buffer Register: VME address H0839
 Channel 1 User 6 Switch Active Buffer Register: VME address H083B
 Channel 1 User 7 Switch Active Buffer Register: VME address H083D
 Channel 1 User 8 Switch Active Buffer Register: VME address H083F
 Channel 2 User 1 Switch Active Buffer Register: VME address H1031
 Channel 2 User 2 Switch Active Buffer Register: VME address H1033
 Channel 2 User 3 Switch Active Buffer Register: VME address H1035
 Channel 2 User 4 Switch Active Buffer Register: VME address H1037
 Channel 2 User 5 Switch Active Buffer Register: VME address H1039
 Channel 2 User 6 Switch Active Buffer Register: VME address H103B
 Channel 2 User 7 Switch Active Buffer Register: VME address H103D
 Channel 2 User 8 Switch Active Buffer Register: VME address H103F
 Channel 3 User 1 Switch Active Buffer Register: VME address H1831
 Channel 3 User 2 Switch Active Buffer Register: VME address H1833
 Channel 3 User 3 Switch Active Buffer Register: VME address H1835
 Channel 3 User 4 Switch Active Buffer Register: VME address H1837
 Channel 3 User 5 Switch Active Buffer Register: VME address H1839
 Channel 3 User 6 Switch Active Buffer Register: VME address H183B
 Channel 3 User 7 Switch Active Buffer Register: VME address H183D
 Channel 3 User 8 Switch Active Buffer Register: VME address H183F
 Channel 4 User 1 Switch Active Buffer Register: VME address H2031
 Channel 4 User 2 Switch Active Buffer Register: VME address H2033
 Channel 4 User 3 Switch Active Buffer Register: VME address H2035
 Channel 4 User 4 Switch Active Buffer Register: VME address H2037
 Channel 4 User 5 Switch Active Buffer Register: VME address H2039
 Channel 4 User 6 Switch Active Buffer Register: VME address H203B
 Channel 4 User 7 Switch Active Buffer Register: VME address H203D
 Channel 4 User 8 Switch Active Buffer Register: VME address H203F

D7	D6	D5	D4	D3	D2	D1	D0
Z	Z	Z	Z	Z	Z	Z	1/0

D0 1 = Switch Setpoint buffer at Group End, 0 = no switch

The active and inactive Readback buffers are switched at every Group End event. Setpoint buffers will only switch at Group End if commanded to do so, by setting D0 in the appropriate Channel X User X Switch Active Buffer register. When the Group End event occurs, the selected Setpoint buffers are switched, and the Channel X User X Switch Active Buffer registers are cleared. The switching of buffers across boards can be synchronized by using the Switch Buffer Ready register.

Channel X Start Delays

Every user of every channel has a programmable Start delay value. The delays are actually stored in FPGA RAM, but this document refers to delay registers. After the programmable Start delay expires, an additional built-in 100us delay is added. The built-in 100us delay is fixed, and cannot be removed. It allows a PSI enough time to finish sending its response to any previously transmitted Setpoint if the programmable Start delay was zero. No Setpoints are ever transmitted during a Start delay, even if a function is re-started.

Channel X User 1 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 1 Start Delay Upper Register: VME address H0841
 Channel 2 User 1 Start Delay Upper Register: VME address H1041
 Channel 3 User 1 Start Delay Upper Register: VME address H1841
 Channel 4 User 1 Start Delay Upper Register: VME address H2041

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 1 Start delay

Channel X User 1 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 1 Start Delay Lower Register: VME address H0842 -> H0843
 Channel 2 User 1 Start Delay Lower Register: VME address H1042 -> H1043
 Channel 3 User 1 Start Delay Lower Register: VME address H1842 -> H1843
 Channel 4 User 1 Start Delay Lower Register: VME address H2042 -> H2043

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 1 Start delay

The Channel X User 1 Start Delay Upper register and Channel X User 1 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 2 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 2 Start Delay Upper Register: VME address H0845

Channel 2 User 2 Start Delay Upper Register: VME address H1045

Channel 3 User 2 Start Delay Upper Register: VME address H1845

Channel 4 User 2 Start Delay Upper Register: VME address H2045

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 2 Start delay

Channel X User 2 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 2 Start Delay Lower Register: VME address H0846 -> H0847

Channel 2 User 2 Start Delay Lower Register: VME address H1046 -> H1047

Channel 3 User 2 Start Delay Lower Register: VME address H1846 -> H1847

Channel 4 User 2 Start Delay Lower Register: VME address H2046 -> H2047

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 2 Start delay

The Channel X User 2 Start Delay Upper register and Channel X User 2 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 3 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 3 Start Delay Upper Register: VME address H0849

Channel 2 User 3 Start Delay Upper Register: VME address H1049

Channel 3 User 3 Start Delay Upper Register: VME address H1849

Channel 4 User 3 Start Delay Upper Register: VME address H2049

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 3 Start delay

Channel X User 3 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 3 Start Delay Lower Register: VME address H084A -> H084B

Channel 2 User 3 Start Delay Lower Register: VME address H104A -> H104B

Channel 3 User 3 Start Delay Lower Register: VME address H184A -> H184B

Channel 4 User 3 Start Delay Lower Register: VME address H204A -> H204B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 3 Start delay

The Channel X User 3 Start Delay Upper register and Channel X User 3 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 4 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 4 Start Delay Upper Register: VME address H084D

Channel 2 User 4 Start Delay Upper Register: VME address H104D

Channel 3 User 4 Start Delay Upper Register: VME address H184D

Channel 4 User 4 Start Delay Upper Register: VME address H204D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 4 Start delay

Channel X User 4 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 4 Start Delay Lower Register: VME address H084E -> H084F

Channel 2 User 4 Start Delay Lower Register: VME address H104E -> H104F

Channel 3 User 4 Start Delay Lower Register: VME address H184E -> H184F

Channel 4 User 4 Start Delay Lower Register: VME address H204E -> H204F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 4 Start delay

The Channel X User 4 Start Delay Upper register and Channel X User 4 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 5 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 5 Start Delay Upper Register: VME address H0851

Channel 2 User 5 Start Delay Upper Register: VME address H1051

Channel 3 User 5 Start Delay Upper Register: VME address H1851

Channel 4 User 5 Start Delay Upper Register: VME address H2051

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 5 Start delay

Channel X User 5 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 5 Start Delay Lower Register: VME address H0852 -> H0853

Channel 2 User 5 Start Delay Lower Register: VME address H1052 -> H1053

Channel 3 User 5 Start Delay Lower Register: VME address H1852 -> H1853

Channel 4 User 5 Start Delay Lower Register: VME address H2052 -> H2053

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 5 Start delay

The Channel X User 5 Start Delay Upper register and Channel X User 5 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 6 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 6 Start Delay Upper Register: VME address H0855

Channel 2 User 6 Start Delay Upper Register: VME address H1055

Channel 3 User 6 Start Delay Upper Register: VME address H1855

Channel 4 User 6 Start Delay Upper Register: VME address H2055

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 6 Start delay

Channel X User 6 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 6 Start Delay Lower Register: VME address H0856 -> H0857

Channel 2 User 6 Start Delay Lower Register: VME address H1056 -> H1057

Channel 3 User 6 Start Delay Lower Register: VME address H1856 -> H1857

Channel 4 User 6 Start Delay Lower Register: VME address H2056 -> H2057

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 6 Start delay

The Channel X User 6 Start Delay Upper register and Channel X User 6 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 7 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 7 Start Delay Upper Register: VME address H0859

Channel 2 User 7 Start Delay Upper Register: VME address H1059

Channel 3 User 7 Start Delay Upper Register: VME address H1859

Channel 4 User 7 Start Delay Upper Register: VME address H2059

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 7 Start delay

Channel X User 7 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 7 Start Delay Lower Register: VME address H085A -> H085B

Channel 2 User 7 Start Delay Lower Register: VME address H105A -> H105B

Channel 3 User 7 Start Delay Lower Register: VME address H185A -> H185B

Channel 4 User 7 Start Delay Lower Register: VME address H205A -> H205B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 7 Start delay

The Channel X User 7 Start Delay Upper register and Channel X User 7 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 8 Start Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 8 Start Delay Upper Register: VME address H085D

Channel 2 User 8 Start Delay Upper Register: VME address H105D

Channel 3 User 8 Start Delay Upper Register: VME address H185D

Channel 4 User 8 Start Delay Upper Register: VME address H205D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 8 Start delay

Channel X User 8 Start Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 8 Start Delay Lower Register: VME address H085E -> H085F

Channel 2 User 8 Start Delay Lower Register: VME address H105E -> H105F

Channel 3 User 8 Start Delay Lower Register: VME address H185E -> H185F

Channel 4 User 8 Start Delay Lower Register: VME address H205E -> H205F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 8 Start delay

The Channel X User 8 Start Delay Upper register and Channel X User 8 Start Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Start event. When the counter reaches zero, the first Setpoint is sent.

Channel X Resume 1 Delays

Every user of every channel has a programmable Resume 1 delay value. The delays are actually stored in FPGA RAM, but this document refers to delay registers. After the programmable Resume 1 delay expires, an additional built-in 100us delay is added. The built-in 100us delay is fixed, and cannot be removed. It allows a PSI enough time to finish sending its response to any previously transmitted Setpoint. Setpoints will be sent during the programmable Resume 1 delay, but not during the built-in delay.

Channel X User 1 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 1 Resume 1 Delay Upper Register: VME address H0861

Channel 2 User 1 Resume 1 Delay Upper Register: VME address H1061

Channel 3 User 1 Resume 1 Delay Upper Register: VME address H1861

Channel 4 User 1 Resume 1 Delay Upper Register: VME address H2061

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 1 Resume 1 delay

Channel X User 1 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 1 Resume 1 Delay Lower Register: VME address H0862 -> H0863

Channel 2 User 1 Resume 1 Delay Lower Register: VME address H1062 -> H1063

Channel 3 User 1 Resume 1 Delay Lower Register: VME address H1862 -> H1863

Channel 4 User 1 Resume 1 Delay Lower Register: VME address H2062 -> H2063

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 1 Resume 1 delay

The Channel X User 1 Resume 1 Delay Upper register and Channel X User 1 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 2 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 2 Resume 1 Delay Upper Register: VME address H0865

Channel 2 User 2 Resume 1 Delay Upper Register: VME address H1065

Channel 3 User 2 Resume 1 Delay Upper Register: VME address H1865

Channel 4 User 2 Resume 1 Delay Upper Register: VME address H2065

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 2 Resume 1 delay

Channel X User 2 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 2 Resume 1 Delay Lower Register: VME address H0866 -> H0867

Channel 2 User 2 Resume 1 Delay Lower Register: VME address H1066 -> H1067

Channel 3 User 2 Resume 1 Delay Lower Register: VME address H1866 -> H1867

Channel 4 User 2 Resume 1 Delay Lower Register: VME address H2066 -> H2067

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 2 Resume 1 delay

The Channel X User 2 Resume 1 Delay Upper register and Channel X User 2 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 3 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 3 Resume 1 Delay Upper Register: VME address H0869

Channel 2 User 3 Resume 1 Delay Upper Register: VME address H1069

Channel 3 User 3 Resume 1 Delay Upper Register: VME address H1869

Channel 4 User 3 Resume 1 Delay Upper Register: VME address H2069

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 3 Resume 1 delay

Channel X User 3 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 3 Resume 1 Delay Lower Register: VME address H086A -> H086B

Channel 2 User 3 Resume 1 Delay Lower Register: VME address H106A -> H106B

Channel 3 User 3 Resume 1 Delay Lower Register: VME address H186A -> H186B

Channel 4 User 3 Resume 1 Delay Lower Register: VME address H206A -> H206B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 3 Resume 1 delay

The Channel X User 3 Resume 1 Delay Upper register and Channel X User 3 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 4 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 4 Resume 1 Delay Upper Register: VME address H086D

Channel 2 User 4 Resume 1 Delay Upper Register: VME address H106D

Channel 3 User 4 Resume 1 Delay Upper Register: VME address H186D

Channel 4 User 4 Resume 1 Delay Upper Register: VME address H206D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 4 Resume 1 delay

Channel X User 4 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 4 Resume 1 Delay Lower Register: VME address H086E -> H086F

Channel 2 User 4 Resume 1 Delay Lower Register: VME address H106E -> H106F

Channel 3 User 4 Resume 1 Delay Lower Register: VME address H186E -> H186F

Channel 4 User 4 Resume 1 Delay Lower Register: VME address H206E -> H206F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 4 Resume 1 delay

The Channel X User 4 Resume 1 Delay Upper register and Channel X User 4 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 5 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 5 Resume 1 Delay Upper Register: VME address H0871

Channel 2 User 5 Resume 1 Delay Upper Register: VME address H1071

Channel 3 User 5 Resume 1 Delay Upper Register: VME address H1871

Channel 4 User 5 Resume 1 Delay Upper Register: VME address H2071

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 5 Resume 1 delay

Channel X User 5 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 5 Resume 1 Delay Lower Register: VME address H0872 -> H0873

Channel 2 User 5 Resume 1 Delay Lower Register: VME address H1072 -> H1073

Channel 3 User 5 Resume 1 Delay Lower Register: VME address H1872 -> H1873

Channel 4 User 5 Resume 1 Delay Lower Register: VME address H2072 -> H2073

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 5 Resume 1 delay

The Channel X User 5 Resume 1 Delay Upper register and Channel X User 5 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 6 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 6 Resume 1 Delay Upper Register: VME address H0875

Channel 2 User 6 Resume 1 Delay Upper Register: VME address H1075

Channel 3 User 6 Resume 1 Delay Upper Register: VME address H1875

Channel 4 User 6 Resume 1 Delay Upper Register: VME address H2075

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 6 Resume 1 delay

Channel X User 6 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 6 Resume 1 Delay Lower Register: VME address H0876 -> H0877

Channel 2 User 6 Resume 1 Delay Lower Register: VME address H1076 -> H1077

Channel 3 User 6 Resume 1 Delay Lower Register: VME address H1876 -> H1877

Channel 4 User 6 Resume 1 Delay Lower Register: VME address H2076 -> H2077

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 6 Resume 1 delay

The Channel X User 6 Resume 1 Delay Upper register and Channel X User 6 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 7 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 7 Resume 1 Delay Upper Register: VME address H0879

Channel 2 User 7 Resume 1 Delay Upper Register: VME address H1079

Channel 3 User 7 Resume 1 Delay Upper Register: VME address H1879

Channel 4 User 7 Resume 1 Delay Upper Register: VME address H2079

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 7 Resume 1 delay

Channel X User 7 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 7 Resume 1 Delay Lower Register: VME address H087A -> H087B

Channel 2 User 7 Resume 1 Delay Lower Register: VME address H107A -> H107B

Channel 3 User 7 Resume 1 Delay Lower Register: VME address H187A -> H187B

Channel 4 User 7 Resume 1 Delay Lower Register: VME address H207A -> H207B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 7 Resume 1 delay

The Channel X User 7 Resume 1 Delay Upper register and Channel X User 7 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 8 Resume 1 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 8 Resume 1 Delay Upper Register: VME address H087D

Channel 2 User 8 Resume 1 Delay Upper Register: VME address H107D

Channel 3 User 8 Resume 1 Delay Upper Register: VME address H187D

Channel 4 User 8 Resume 1 Delay Upper Register: VME address H207D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 8 Resume 1 delay

Channel X User 8 Resume 1 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 8 Resume 1 Delay Lower Register: VME address H087E -> H087F

Channel 2 User 8 Resume 1 Delay Lower Register: VME address H107E -> H107F

Channel 3 User 8 Resume 1 Delay Lower Register: VME address H187E -> H187F

Channel 4 User 8 Resume 1 Delay Lower Register: VME address H207E -> H207F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 8 Resume 1 delay

The Channel X User 8 Resume 1 Delay Upper register and Channel X User 8 Resume 1 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 1 event. When the counter reaches zero, the next Setpoint is sent.

Channel X Resume 2 Delays

Every user of every channel has a programmable Resume 2 delay value. The delays are actually stored in FPGA RAM, but this document refers to delay registers. After the programmable Resume 2 delay expires, an additional built-in 100us delay is added. The built-in 100us delay is fixed, and cannot be removed. It allows a PSI enough time to finish sending its response to any previously transmitted Setpoint. Setpoints will be sent during the programmable Resume 2 delay, but not during the built-in delay.

Channel X User 1 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 1 Resume 2 Delay Upper Register: VME address H0881

Channel 2 User 1 Resume 2 Delay Upper Register: VME address H1081

Channel 3 User 1 Resume 2 Delay Upper Register: VME address H1881

Channel 4 User 1 Resume 2 Delay Upper Register: VME address H2081

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 1 Resume 2 delay

Channel X User 1 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 1 Resume 2 Delay Lower Register: VME address H0882 -> H0883

Channel 2 User 1 Resume 2 Delay Lower Register: VME address H1082 -> H1083

Channel 3 User 1 Resume 2 Delay Lower Register: VME address H1882 -> H1883

Channel 4 User 1 Resume 2 Delay Lower Register: VME address H2082 -> H2083

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 1 Resume 2 delay

The Channel X User 1 Resume 2 Delay Upper register and Channel X User 1 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 2 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 2 Resume 2 Delay Upper Register: VME address H0885

Channel 2 User 2 Resume 2 Delay Upper Register: VME address H1085

Channel 3 User 2 Resume 2 Delay Upper Register: VME address H1885

Channel 4 User 2 Resume 2 Delay Upper Register: VME address H2085

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 2 Resume 2 delay

Channel X User 2 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 2 Resume 2 Delay Lower Register: VME address H0886 -> H0887

Channel 2 User 2 Resume 2 Delay Lower Register: VME address H1086 -> H1087

Channel 3 User 2 Resume 2 Delay Lower Register: VME address H1886 -> H1887

Channel 4 User 2 Resume 2 Delay Lower Register: VME address H2086 -> H2087

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 2 Resume 2 delay

The Channel X User 2 Resume 2 Delay Upper register and Channel X User 2 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 3 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 3 Resume 2 Delay Upper Register: VME address H0889

Channel 2 User 3 Resume 2 Delay Upper Register: VME address H1089

Channel 3 User 3 Resume 2 Delay Upper Register: VME address H1889

Channel 4 User 3 Resume 2 Delay Upper Register: VME address H2089

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 3 Resume 2 delay

Channel X User 3 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 3 Resume 2 Delay Lower Register: VME address H088A -> H088B

Channel 2 User 3 Resume 2 Delay Lower Register: VME address H108A -> H108B

Channel 3 User 3 Resume 2 Delay Lower Register: VME address H188A -> H188B

Channel 4 User 3 Resume 2 Delay Lower Register: VME address H208A -> H208B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 3 Resume 2 delay

The Channel X User 3 Resume 2 Delay Upper register and Channel X User 3 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 4 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 4 Resume 2 Delay Upper Register: VME address H088D

Channel 2 User 4 Resume 2 Delay Upper Register: VME address H108D

Channel 3 User 4 Resume 2 Delay Upper Register: VME address H188D

Channel 4 User 4 Resume 2 Delay Upper Register: VME address H208D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 4 Resume 2 delay

Channel X User 4 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 4 Resume 2 Delay Lower Register: VME address H088E -> H088F

Channel 2 User 4 Resume 2 Delay Lower Register: VME address H108E -> H108F

Channel 3 User 4 Resume 2 Delay Lower Register: VME address H188E -> H188F

Channel 4 User 4 Resume 2 Delay Lower Register: VME address H208E -> H208F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 4 Resume 2 delay

The Channel X User 4 Resume 2 Delay Upper register and Channel X User 4 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 5 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 5 Resume 2 Delay Upper Register: VME address H0891

Channel 2 User 5 Resume 2 Delay Upper Register: VME address H1091

Channel 3 User 5 Resume 2 Delay Upper Register: VME address H1891

Channel 4 User 5 Resume 2 Delay Upper Register: VME address H2091

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 5 Resume 2 delay

Channel X User 5 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 5 Resume 2 Delay Lower Register: VME address H0892 -> H0893

Channel 2 User 5 Resume 2 Delay Lower Register: VME address H1092 -> H1093

Channel 3 User 5 Resume 2 Delay Lower Register: VME address H1892 -> H1893

Channel 4 User 5 Resume 2 Delay Lower Register: VME address H2092 -> H2093

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 5 Resume 2 delay

The Channel X User 5 Resume 2 Delay Upper register and Channel X User 5 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 6 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 6 Resume 2 Delay Upper Register: VME address H0895

Channel 2 User 6 Resume 2 Delay Upper Register: VME address H1095

Channel 3 User 6 Resume 2 Delay Upper Register: VME address H1895

Channel 4 User 6 Resume 2 Delay Upper Register: VME address H2095

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 6 Resume 2 delay

Channel X User 6 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 6 Resume 2 Delay Lower Register: VME address H0896 -> H0897

Channel 2 User 6 Resume 2 Delay Lower Register: VME address H1096 -> H1097

Channel 3 User 6 Resume 2 Delay Lower Register: VME address H1896 -> H1897

Channel 4 User 6 Resume 2 Delay Lower Register: VME address H2096 -> H2097

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 6 Resume 2 delay

The Channel X User 6 Resume 2 Delay Upper register and Channel X User 6 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 7 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 7 Resume 2 Delay Upper Register: VME address H0899

Channel 2 User 7 Resume 2 Delay Upper Register: VME address H1099

Channel 3 User 7 Resume 2 Delay Upper Register: VME address H1899

Channel 4 User 7 Resume 2 Delay Upper Register: VME address H2099

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 7 Resume 2 delay

Channel X User 7 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 7 Resume 2 Delay Lower Register: VME address H089A -> H089B

Channel 2 User 7 Resume 2 Delay Lower Register: VME address H109A -> H109B

Channel 3 User 7 Resume 2 Delay Lower Register: VME address H189A -> H189B

Channel 4 User 7 Resume 2 Delay Lower Register: VME address H209A -> H209B

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 7 Resume 2 delay

The Channel X User 7 Resume 2 Delay Upper register and Channel X User 7 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 8 Resume 2 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 8 Resume 2 Delay Upper Register: VME address H089D

Channel 2 User 8 Resume 2 Delay Upper Register: VME address H109D

Channel 3 User 8 Resume 2 Delay Upper Register: VME address H189D

Channel 4 User 8 Resume 2 Delay Upper Register: VME address H209D

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 8 Resume 2 delay

Channel X User 8 Resume 2 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 8 Resume 2 Delay Lower Register: VME address H089E -> H089F

Channel 2 User 8 Resume 2 Delay Lower Register: VME address H109E -> H109F

Channel 3 User 8 Resume 2 Delay Lower Register: VME address H189E -> H189F

Channel 4 User 8 Resume 2 Delay Lower Register: VME address H209E -> H209F

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 8 Resume 2 delay

The Channel X User 8 Resume 2 Delay Upper register and Channel X User 8 Resume 2 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 2 event. When the counter reaches zero, the next Setpoint is sent.

Channel X Resume 3 Delays

Every user of every channel has a programmable Resume 3 delay value. The delays are actually stored in FPGA RAM, but this document refers to delay registers. After the programmable Resume 3 delay expires, an additional built-in 100us delay is added. The built-in 100us delay is fixed, and cannot be removed. It allows a PSI enough time to finish sending its response to any previously transmitted Setpoint. Setpoints will be sent during the programmable Resume 3 delay, but not during the built-in delay.

Channel X User 1 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 1 Resume 3 Delay Upper Register: VME address H08A1

Channel 2 User 1 Resume 3 Delay Upper Register: VME address H10A1

Channel 3 User 1 Resume 3 Delay Upper Register: VME address H18A1

Channel 4 User 1 Resume 3 Delay Upper Register: VME address H20A1

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 1 Resume 3 delay

Channel X User 1 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 1 Resume 3 Delay Lower Register: VME address H08A2 -> H08A3

Channel 2 User 1 Resume 3 Delay Lower Register: VME address H10A2 -> H10A3

Channel 3 User 1 Resume 3 Delay Lower Register: VME address H18A2 -> H18A3

Channel 4 User 1 Resume 3 Delay Lower Register: VME address H20A2 -> H20A3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 1 Resume 3 delay

The Channel X User 1 Resume 3 Delay Upper register and Channel X User 1 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 2 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 2 Resume 3 Delay Upper Register: VME address H08A5
 Channel 2 User 2 Resume 3 Delay Upper Register: VME address H10A5
 Channel 3 User 2 Resume 3 Delay Upper Register: VME address H18A5
 Channel 4 User 2 Resume 3 Delay Upper Register: VME address H20A5

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 2 Resume 3 delay

Channel X User 2 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 2 Resume 3 Delay Lower Register: VME address H08A6 -> H08A7
 Channel 2 User 2 Resume 3 Delay Lower Register: VME address H10A6 -> H10A7
 Channel 3 User 2 Resume 3 Delay Lower Register: VME address H18A6 -> H18A7
 Channel 4 User 2 Resume 3 Delay Lower Register: VME address H20A6 -> H20A7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 2 Resume 3 delay

The Channel X User 2 Resume 3 Delay Upper register and Channel X User 2 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 3 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 3 Resume 3 Delay Upper Register: VME address H08A9

Channel 2 User 3 Resume 3 Delay Upper Register: VME address H10A9

Channel 3 User 3 Resume 3 Delay Upper Register: VME address H18A9

Channel 4 User 3 Resume 3 Delay Upper Register: VME address H20A9

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 3 Resume 3 delay

Channel X User 3 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 3 Resume 3 Delay Lower Register: VME address H08AA -> H08AB

Channel 2 User 3 Resume 3 Delay Lower Register: VME address H10AA -> H10AB

Channel 3 User 3 Resume 3 Delay Lower Register: VME address H18AA -> H18AB

Channel 4 User 3 Resume 3 Delay Lower Register: VME address H20AA -> H20AB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 3 Resume 3 delay

The Channel X User 3 Resume 3 Delay Upper register and Channel X User 3 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 4 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 4 Resume 3 Delay Upper Register: VME address H08AD

Channel 2 User 4 Resume 3 Delay Upper Register: VME address H10AD

Channel 3 User 4 Resume 3 Delay Upper Register: VME address H18AD

Channel 4 User 4 Resume 3 Delay Upper Register: VME address H20AD

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 4 Resume 2 delay

Channel X User 4 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 4 Resume 3 Delay Lower Register: VME address H08AE -> H08AF

Channel 2 User 4 Resume 3 Delay Lower Register: VME address H10AE -> H10AF

Channel 3 User 4 Resume 3 Delay Lower Register: VME address H18AE -> H18AF

Channel 4 User 4 Resume 3 Delay Lower Register: VME address H20AE -> H20AF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 4 Resume 3 delay

The Channel X User 4 Resume 3 Delay Upper register and Channel X User 4 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 5 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 5 Resume 3 Delay Upper Register: VME address H08B1

Channel 2 User 5 Resume 3 Delay Upper Register: VME address H10B1

Channel 3 User 5 Resume 3 Delay Upper Register: VME address H18B1

Channel 4 User 5 Resume 3 Delay Upper Register: VME address H20B1

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 5 Resume 3 delay

Channel X User 5 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 5 Resume 3 Delay Lower Register: VME address H08B2 -> H08B3

Channel 2 User 5 Resume 3 Delay Lower Register: VME address H10B2 -> H10B3

Channel 3 User 5 Resume 3 Delay Lower Register: VME address H18B2 -> H18B3

Channel 4 User 5 Resume 3 Delay Lower Register: VME address H20B2 -> H20B3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 5 Resume 3 delay

The Channel X User 5 Resume 3 Delay Upper register and Channel X User 5 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 6 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 6 Resume 3 Delay Upper Register: VME address H08B5

Channel 2 User 6 Resume 3 Delay Upper Register: VME address H10B5

Channel 3 User 6 Resume 3 Delay Upper Register: VME address H18B5

Channel 4 User 6 Resume 3 Delay Upper Register: VME address H20B5

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 6 Resume 3 delay

Channel X User 6 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 6 Resume 3 Delay Lower Register: VME address H08B6 -> H08B7

Channel 2 User 6 Resume 3 Delay Lower Register: VME address H10B6 -> H10B7

Channel 3 User 6 Resume 3 Delay Lower Register: VME address H18B6 -> H18B7

Channel 4 User 6 Resume 3 Delay Lower Register: VME address H20B6 -> H20B7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 6 Resume 3 delay

The Channel X User 6 Resume 3 Delay Upper register and Channel X User 6 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 7 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 7 Resume 3 Delay Upper Register: VME address H08B9

Channel 2 User 7 Resume 3 Delay Upper Register: VME address H10B9

Channel 3 User 7 Resume 3 Delay Upper Register: VME address H18B9

Channel 4 User 7 Resume 3 Delay Upper Register: VME address H20B9

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 7 Resume 3 delay

Channel X User 7 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 7 Resume 3 Delay Lower Register: VME address H08BA -> H08BB

Channel 2 User 7 Resume 3 Delay Lower Register: VME address H10BA -> H10BB

Channel 3 User 7 Resume 3 Delay Lower Register: VME address H18BA -> H18BB

Channel 4 User 7 Resume 3 Delay Lower Register: VME address H20BA -> H20BB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 7 Resume 3 delay

The Channel X User 7 Resume 3 Delay Upper register and Channel X User 7 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 8 Resume 3 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 8 Resume 3 Delay Upper Register: VME address H08BD

Channel 2 User 8 Resume 3 Delay Upper Register: VME address H10BD

Channel 3 User 8 Resume 3 Delay Upper Register: VME address H18BD

Channel 4 User 8 Resume 3 Delay Upper Register: VME address H20BD

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 8 Resume 3 delay

Channel X User 8 Resume 3 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 8 Resume 3 Delay Lower Register: VME address H08BE -> H08BF

Channel 2 User 8 Resume 3 Delay Lower Register: VME address H10BE -> H10BF

Channel 3 User 8 Resume 3 Delay Lower Register: VME address H18BE -> H18BF

Channel 4 User 8 Resume 3 Delay Lower Register: VME address H20BE -> H20BF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 8 Resume 3 delay

The Channel X User 8 Resume 3 Delay Upper register and Channel X User 8 Resume 3 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 3 event. When the counter reaches zero, the next Setpoint is sent.

Channel X Resume 4 Delays

Every user of every channel has a programmable Resume 4 delay value. The delays are actually stored in FPGA RAM, but this document refers to delay registers. After the programmable Resume 4 delay expires, an additional built-in 100us delay is added. The built-in 100us delay is fixed, and cannot be removed. It allows a PSI enough time to finish sending its response to any previously transmitted Setpoint. Setpoints will be sent during the programmable Resume 4 delay, but not during the built-in delay.

Channel X User 1 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 1 Resume 4 Delay Upper Register: VME address H08C1

Channel 2 User 1 Resume 4 Delay Upper Register: VME address H10C1

Channel 3 User 1 Resume 4 Delay Upper Register: VME address H18C1

Channel 4 User 1 Resume 4 Delay Upper Register: VME address H20C1

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 1 Resume 4 delay

Channel X User 1 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 1 Resume 4 Delay Lower Register: VME address H08C2 -> H08C3

Channel 2 User 1 Resume 4 Delay Lower Register: VME address H10C2 -> H10C3

Channel 3 User 1 Resume 4 Delay Lower Register: VME address H18C2 -> H18C3

Channel 4 User 1 Resume 4 Delay Lower Register: VME address H20C2 -> H20C3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 1 Resume 4 delay

The Channel X User 1 Resume 4 Delay Upper register and Channel X User 1 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 2 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 2 Resume 4 Delay Upper Register: VME address H08C5

Channel 2 User 2 Resume 4 Delay Upper Register: VME address H10C5

Channel 3 User 2 Resume 4 Delay Upper Register: VME address H18C5

Channel 4 User 2 Resume 4 Delay Upper Register: VME address H20C5

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 2 Resume 4 delay

Channel X User 2 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 2 Resume 4 Delay Lower Register: VME address H08C6 -> H08C7

Channel 2 User 2 Resume 4 Delay Lower Register: VME address H10C6 -> H10C7

Channel 3 User 2 Resume 4 Delay Lower Register: VME address H18C6 -> H18C7

Channel 4 User 2 Resume 4 Delay Lower Register: VME address H20C6 -> H20C7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 2 Resume 4 delay

The Channel X User 2 Resume 4 Delay Upper register and Channel X User 2 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 3 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 3 Resume 4 Delay Upper Register: VME address H08C9

Channel 2 User 3 Resume 4 Delay Upper Register: VME address H10C9

Channel 3 User 3 Resume 4 Delay Upper Register: VME address H18C9

Channel 4 User 3 Resume 4 Delay Upper Register: VME address H20C9

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 3 Resume 4 delay

Channel X User 3 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 3 Resume 4 Delay Lower Register: VME address H08CA -> H08CB

Channel 2 User 3 Resume 4 Delay Lower Register: VME address H10CA -> H10CB

Channel 3 User 3 Resume 4 Delay Lower Register: VME address H18CA -> H18CB

Channel 4 User 3 Resume 4 Delay Lower Register: VME address H20CA -> H20CB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 3 Resume 4 delay

The Channel X User 3 Resume 4 Delay Upper register and Channel X User 3 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 4 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 4 Resume 4 Delay Upper Register: VME address H08CD

Channel 2 User 4 Resume 4 Delay Upper Register: VME address H10CD

Channel 3 User 4 Resume 4 Delay Upper Register: VME address H18CD

Channel 4 User 4 Resume 4 Delay Upper Register: VME address H20CD

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 4 Resume 4 delay

Channel X User 4 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 4 Resume 4 Delay Lower Register: VME address H08CE -> H08CF

Channel 2 User 4 Resume 4 Delay Lower Register: VME address H10CE -> H10CF

Channel 3 User 4 Resume 4 Delay Lower Register: VME address H18CE -> H18CF

Channel 4 User 4 Resume 4 Delay Lower Register: VME address H20CE -> H20CF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 4 Resume 4 delay

The Channel X User 4 Resume 4 Delay Upper register and Channel X User 4 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 5 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 5 Resume 4 Delay Upper Register: VME address H08D1

Channel 2 User 5 Resume 4 Delay Upper Register: VME address H10D1

Channel 3 User 5 Resume 4 Delay Upper Register: VME address H18D1

Channel 4 User 5 Resume 4 Delay Upper Register: VME address H20D1

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 5 Resume 4 delay

Channel X User 5 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 5 Resume 4 Delay Lower Register: VME address H08D2 -> H08D3

Channel 2 User 5 Resume 4 Delay Lower Register: VME address H10D2 -> H10D3

Channel 3 User 5 Resume 4 Delay Lower Register: VME address H18D2 -> H18D3

Channel 4 User 5 Resume 4 Delay Lower Register: VME address H20D2 -> H20D3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 5 Resume 4 delay

The Channel X User 5 Resume 4 Delay Upper register and Channel X User 5 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 6 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 6 Resume 4 Delay Upper Register: VME address H08D5

Channel 2 User 6 Resume 4 Delay Upper Register: VME address H10D5

Channel 3 User 6 Resume 4 Delay Upper Register: VME address H18D5

Channel 4 User 6 Resume 4 Delay Upper Register: VME address H20D5

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 6 Resume 4 delay

Channel X User 6 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 6 Resume 4 Delay Lower Register: VME address H08D6 -> H08D7

Channel 2 User 6 Resume 4 Delay Lower Register: VME address H10D6 -> H10D7

Channel 3 User 6 Resume 4 Delay Lower Register: VME address H18D6 -> H18D7

Channel 4 User 6 Resume 4 Delay Lower Register: VME address H20D6 -> H20D7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 6 Resume 4 delay

The Channel X User 6 Resume 4 Delay Upper register and Channel X User 6 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 7 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 7 Resume 4 Delay Upper Register: VME address H08D9

Channel 2 User 7 Resume 4 Delay Upper Register: VME address H10D9

Channel 3 User 7 Resume 4 Delay Upper Register: VME address H18D9

Channel 4 User 7 Resume 4 Delay Upper Register: VME address H20D9

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 7 Resume 4 delay

Channel X User 7 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 7 Resume 4 Delay Lower Register: VME address H08DA -> H08DB

Channel 2 User 7 Resume 4 Delay Lower Register: VME address H10DA -> H10DB

Channel 3 User 7 Resume 4 Delay Lower Register: VME address H18DA -> H18DB

Channel 4 User 7 Resume 4 Delay Lower Register: VME address H20DA -> H20DB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 7 Resume 4 delay

The Channel X User 7 Resume 4 Delay Upper register and Channel X User 7 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Appendix B - V233 Register And Memory Descriptions

Channel X User 8 Resume 4 Delay Upper Register (Read/Write, 1 byte)

Channel 1 User 8 Resume 4 Delay Upper Register: VME address H08DD

Channel 2 User 8 Resume 4 Delay Upper Register: VME address H10DD

Channel 3 User 8 Resume 4 Delay Upper Register: VME address H18DD

Channel 4 User 8 Resume 4 Delay Upper Register: VME address H20DD

D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D7 -> D0 High 8 bits of 24-bit User 8 Resume 4 delay

Channel X User 8 Resume 4 Delay Lower Register (Read/Write, 2 bytes)

Channel 1 User 8 Resume 4 Delay Lower Register: VME address H08DE -> H08DF

Channel 2 User 8 Resume 4 Delay Lower Register: VME address H10DE -> H10DF

Channel 3 User 8 Resume 4 Delay Lower Register: VME address H18DE -> H18DF

Channel 4 User 8 Resume 4 Delay Lower Register: VME address H20DE -> H20DF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Low 16 bits of 24-bit User 8 Resume 4 delay

The Channel X User 8 Resume 4 Delay Upper register and Channel X User 8 Resume 4 Delay Lower register combine to provide a 24-bit delay value. The delay is loaded into a counter that is clocked by a 1MHz signal. The counter begins to count down upon the occurrence of the Resume 4 event. When the counter reaches zero, the next Setpoint is sent.

Single Frame Registers

The Function Generator is used to send groups of Setpoints, called a function, to a PSI. These Setpoints set a reference voltage in the PSI that is used to control a power supply's output level. Functions are stored in on-board memory, with each setpoint usually containing a Frame ID of 15H. This Frame ID instructs the PSI to return an Echo of the Setpoint, a Status word, and analog inputs ADC1, ADC2, ADC3, and ADC4.

The Function Generator is also capable of sending individual command, setpoint, or read frames to a PSI. The process involves programming the Single Frame registers by setting the Frame ID, Auxiliary bits, and the command or setpoint value itself. All that remains is to actually initiate the transmission by setting D0 in the channel's Send Single Frame register

Currently, only auxiliary bits sent with setpoints are recognized by PSIs. The auxiliary bits sent with commands are ignored.

Individual command, setpoint, or read frames may not be sent during a function. However, they may be sent any time the channel is dis-armed, or be sent automatically 100us after the Group End event occurs.

A command, setpoint, or read frame will generate Readbacks, and they are stored in a special set of registers. The maximum number of Readback words for any frame is 6.

Channel X Single Frame ID Register (Read/Write, 2 bytes)

Channel 1 Single Frame ID Register: VME address H08E0 -> H08E1

Channel 2 Single Frame ID Register: VME address H10E0 -> H10E1

Channel 3 Single Frame ID Register: VME address H18E0 -> H18E1

Channel 4 Single Frame ID Register: VME address H20E0 -> H20E1

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D8 Auxiliary bits 7 -> 0
 D7 -> D0 Frame ID value that defines the frame's purpose
 55H = Setpoint without read
 15H = Setpoint with read
 4AH = Command without read
 0AH = Command with read
 00H = Read Command
 40H = Read Status/ADC

Appendix B - V233 Register And Memory Descriptions

Channel X Single Frame Data Field Register (Read/Write, 2 bytes)

Channel 1 Single Frame Data Field Register: VME address H08E2 -> H08E3

Channel 2 Single Frame Data Field Register: VME address H10E2 -> H10E3

Channel 3 Single Frame Data Field Register: VME address H18E2 -> H18E3

Channel 4 Single Frame Data Field Register: VME address H20E2 -> H20E3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 Command or setpoint value (n/a for read frames)

For setpoint frames, the command is a two's complement binary value written to a DAC. For read frames, the command value is N/A. For command frames, the normal command bit definitions are shown below. However, these bits may vary for different power supplies.

D15 -> D14 00 = power supply off
 01 = power supply standby
 10 = power supply reset
 11 = power supply on

D13 1 = power supply in negative polarity, 0 = normal polarity

D12 -> D0 "Don't Care"

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 1 Register (Read Only, 2 bytes)

Channel 1 Readback ID 1 Register: VME address H08E4

Channel 2 Readback ID 1 Register: VME address H10E4

Channel 3 Readback ID 1 Register: VME address H18E4

Channel 4 Readback ID 1 Register: VME address H20E4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 1st Readback ID value

Channel X Readback Data 1 Register (Read Only, 2 bytes)

Channel 1 Readback Data 1 Register: VME address H08E6 -> H08E7

Channel 2 Readback Data 1 Register: VME address H10E6 -> H10E7

Channel 3 Readback Data 1 Register: VME address H18E6 -> H18E7

Channel 4 Readback Data 1 Register: VME address H20E6 -> H20E7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 1st Readback word (Echo)

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 2 Register (Read Only, 2 bytes)

Channel 1 Readback ID 2 Register: VME address H08E8

Channel 2 Readback ID 2 Register: VME address H10E8

Channel 3 Readback ID 2 Register: VME address H18E8

Channel 4 Readback ID 2 Register: VME address H20E8

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 2nd Readback ID value

Channel X Readback Data 2 Register (Read Only, 2 bytes)

Channel 1 Readback Data 2 Register: VME address H08EA -> H08EB

Channel 2 Readback Data 2 Register: VME address H10EA -> H10EB

Channel 3 Readback Data 2 Register: VME address H18EA -> H18EB

Channel 4 Readback Data 2 Register: VME address H20EA -> H20EB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 2nd Readback word (Status)

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 3 Register (Read Only, 2 bytes)

Channel 1 Readback ID 3 Register: VME address H08EC

Channel 2 Readback ID 3 Register: VME address H10EC

Channel 3 Readback ID 3 Register: VME address H18EC

Channel 4 Readback ID 3 Register: VME address H20EC

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 3rd Readback ID value

Channel X Readback Data 3 Register (Read Only, 2 bytes)

Channel 1 Readback Data 3 Register: VME address H08EE -> H08EF

Channel 2 Readback Data 3 Register: VME address H10EE -> H10EF

Channel 3 Readback Data 3 Register: VME address H18EE -> H18EF

Channel 4 Readback Data 3 Register: VME address H20EE -> H20EF

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 3rd Readback word (ADC1)

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 4 Register (Read Only, 2 bytes)

Channel 1 Readback ID 4 Register: VME address H08F0

Channel 2 Readback ID 4 Register: VME address H10F0

Channel 3 Readback ID 4 Register: VME address H18F0

Channel 4 Readback ID 4 Register: VME address H20F0

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 4th Readback ID value

Channel X Readback Data 4 Register (Read Only, 2 bytes)

Channel 1 Readback Data 4 Register: VME address H08F2 -> H08F3

Channel 2 Readback Data 4 Register: VME address H10F2 -> H10F3

Channel 3 Readback Data 4 Register: VME address H18F2 -> H18F3

Channel 4 Readback Data 4 Register: VME address H20F2 -> H20F3

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 4th Readback word (ADC2)

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 5 Register (Read Only, 2 bytes)

Channel 1 Readback ID 5 Register: VME address H08F4

Channel 2 Readback ID 5 Register: VME address H10F4

Channel 3 Readback ID 5 Register: VME address H18F4

Channel 4 Readback ID 5 Register: VME address H20F4

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 5th Readback ID value

Channel X Readback Data 5 Register (Read Only, 2 bytes)

Channel 1 Readback Data 5 Register: VME address H08F6 -> H08F7

Channel 2 Readback Data 5 Register: VME address H10F6 -> H10F7

Channel 3 Readback Data 5 Register: VME address H18F6 -> H18F7

Channel 4 Readback Data 5 Register: VME address H20F6 -> H20F7

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 5th Readback word (ADC3)

Appendix B - V233 Register And Memory Descriptions

Channel X Readback ID 6 Register (Read Only, 2 bytes)

Channel 1 Readback ID 6 Register: VME address H08F8

Channel 2 Readback ID 6 Register: VME address H10F8

Channel 3 Readback ID 6 Register: VME address H18F8

Channel 4 Readback ID 6 Register: VME address H20F8

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D9 Auxiliary bits 6 -> 0 (Aux bit 7 not stored)

D8 1 = CRC error, 0 = no CRC error

D7 -> D0 6th Readback ID value

Channel X Readback Data 6 Register (Read Only, 2 bytes)

Channel 1 Readback Data 6 Register: VME address H08FA -> H08FB

Channel 2 Readback Data 6 Register: VME address H10FA -> H10FB

Channel 3 Readback Data 6 Register: VME address H18FA -> H18FB

Channel 4 Readback Data 6 Register: VME address H20FA -> H20FB

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0

D15 -> D0 6th Readback word (ADC4)

Channel X Send Single Frame Register (Read/Write, Auto Clear 1 byte)

Channel 1 Send Single Frame Register: VME address H08FD

Channel 2 Send Single Frame Register: VME address H10FD

Channel 3 Send Single Frame Register: VME address H18FD

Channel 4 Send Single Frame Register: VME address H20FD

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	1/0	1/0	1/0

D7 -> D3 "Don't Care"

D2 1 = inhibit Timing Trigger output when sending frame, 0 = enable

D1 1 = send frame at Group End event

D0 0 = send frame when channel dis-armed

There is a 16-bit parallel output (called the Timing Trigger output) from channel 1 and channel 2 available on the P2 connector of the Function Generator that can be used for timing pulses. These parallel outputs are normally updated on every word sent to the PSI. Setting bit D2 prevents the Timing Trigger output from being updated with the data field of the single frame sent to the PSI. Instead, the Timing Trigger output will retain the last value sent.

If D1 is set, the frame will automatically be sent 10us after a Group End event occurs. The 10us delay makes sure the PSI has enough time to finish sending its response for any previous setpoint transmitted prior to the Group End event. The operator should make sure that an ensuing Start command does not occur for at least 20us after the Group End event if sending a single frame in this manner. This will make sure that the PSI has enough time to respond to the single frame.

If D0 is set and the channel is armed, the frame will be sent 10us after the channel is dis-armed. If the channel is already disarmed when D0 is set, the frame will be sent immediately. As soon as the frame is sent, the Send Single Frame register is automatically cleared.

Appendix B - V233 Register And Memory Descriptions

Channel X Readback Count Register (Read Only, 1 byte)

Channel 1 Readback Count Register: VME address H08FF

Channel 2 Readback Count Register: VME address H10FF

Channel 3 Readback Count Register: VME address H18FF

Channel 4 Readback Count Register: VME address H20FF

D7	D6	D5	D4	D3	D2	D1	D0
X	X	X	X	X	1/0	1/0	1/0

D7 -> D3 "Don't Care"

D2 -> D0 Running count of single frame Readback words received

The Readback Count register is cleared each time a single frame is sent. Following the transmission of the single frame, each Readback word received from a PSI causes the counter to increment. The maximum value the counter should reach is 6. The counter allows the operator to know when all the Readback words associated with the single frame have been received. The counter is disabled while a function is being sent.

APPENDIX C

V233 PROGRAMMING INSTRUCTIONS

The V233 module assembly (CA3010014) has 5 onboard FPGAs (U42, U33, U34, U35, and U36) that require programming in order to create the V233 programmed assembly (CA3010042). All 5 FPGAs are the same part number: Altera device EP1K100FC256-1. There are two separate programming files. U42 requires one programming file, while U33, U34, U35, and U36 all use the second programming file. The files are actually downloaded and stored in two separate configuration devices, U32 and U55. They have the same part number, EPC2TC32. U32 holds the program for U42, and U55 holds the program for U33, U34, U35, and U36. Each time the V233 is powered up, the configuration devices load the programs into the FPGAs. U33, U34, U35, and U36 have their program loaded in parallel.

The EPC2TC32 configuration devices are programmed with Altera's ByteBlaster. To program U32, the ByteBlaster is connected to J14 of the V233. (J14 has the word "MAIN" next to it.) To program U55, the ByteBlaster is connected to J15 of the V233. When connecting the ByteBlaster to an onboard programming connector, be sure to line up pin 1 of the ByteBlaster plug with pin 1 of the connector. Pin 1 of the ByteBlaster cable normally has a red stripe.

Follow the instructions below to program U32 of the V233 module.

- 1) Position the V233 module next to the computer. Make sure it is placed on a non-conducting surface.
- 2) Apply 5 volts to the V233 board using a power supply connected through an apparatus such as a VME Debugging Board. The power supply should be able to supply up to 5 amps
- 3) Make sure the ByteBlaster cable assembly is connected properly to the computer.
- 4) Connect the ByteBlaster plug to J14, being careful to line up pin 1 of the plug to pin 1 of the connector.
- 5) Open the Max +II program on the computer.
- 6) From the Max +II menu bar, select "MAX+plus II", and then select "Programmer". (The programmer should open)
- 7) From the Max +II menu bar, select "Options", and then select "Hardware Setup...".
- 8) Make sure the Hardware Type is ByteBlaster(MV), and select "OK".
- 9) From the Max +II menu bar, select "Options", and then select "Programming Options...".
- 10) Make sure the "Verify After Programming" box is checked, and select "OK".
- 11) From the Max +II menu bar, select "File", then select "Project>", then select "Name...".

Appendix D - V233 Test Procedure

- 12) Select the following path and file:
C-ad\Elec-server\erelease\Ags\AGSPLD\controls\pof\ca3010042-1-b.pof.
When the file is highlighted, select “OK”.
- 13) An I/O error message may appear saying that a ca3010042-1-b.* file can't be written, found, or open. This message may be ignored. Select “OK” to continue.
- 14) From the Max +II menu bar, select “JTAG”, and then make sure that the top line, “Multi-Device JTAG Chain”, does not have a check mark next to it. If it does, select the line, which will remove the check mark.
- 15) The programmer should show the following information:
Security Bit (un-checked)
File: ca3010042-1-b.pof
Device: EPC2
Checksum: 00C912C9
- 16) Select the “Program” button on the programmer.
- 17) Another I/O error message may appear saying that a ca3010042-1-b.* file can't be written, found, or open. This message may be ignored. Select “OK” to continue.
- 18) Watch the programmer program the device, then verify the program.
- 19) When the device is programmed, a “Programming Complete” message will appear. Select “OK”.

Continue on to program U55.

- 20) Remove the ByteBlaster plug from J14.
- 21) Connect the ByteBlaster plug to J15.
- 22) From the Max +II menu bar, select “File”, then select “Project>”, then select “Name...”.
- 23) Select the following path and file:
C-ad\ Elec-server\erelease\Ags\AGSPLD\controls\pof \ ca3010042-2-c.pof.
When the file is highlighted, select “OK”.
- 24) An I/O error message may appear saying that a ca3010042-2-c.* file can't be written, found, or open. This message may be ignored. Select “OK” to continue.
- 25) From the Max +II menu bar, select “JTAG”, and then make sure that the top line, “Multi-Device JTAG Chain”, does not have a check mark next to it. If it does, select the line, which will remove the check mark.
- 26) The programmer should show the following information:
Security Bit (un-checked)
File: ca3010042-2-c.pof
Device: EPC2
Checksum: 00D7AE89
- 27) Select the “Program” button on the programmer.
- 28) Another I/O error message may appear saying that a ca3010042-2-c.* file can't be written, found, or open. This message may be ignored. Select “OK” to continue.

Appendix D - V233 Test Procedure

- 29) Watch the programmer program the device, then verify the program.
- 30) When the device is programmed, a “Programming Complete” message will appear. Select “OK”.
- 31) Remove the ByteBlaster plug from J15.
- 32) Cycle power to the V233. This will cause the firmware to be loaded from the EPC2s into the gate arrays. Observe that the current draw is approximately 3.5 amps.
- 33) Turn off the power supply, and disconnect it from the board.

The V233 module is now ready for operation. Before being used, appropriate labels should be placed on both Altera configuration devices. Also, solder the necessary bus wires into the board’s Serial Number (J12) and Revision (J13) jumpers.

Note! The FPGAs are reprogrammed each time power is applied. With no VME transfers occurring and with the Event Link disconnected, only the Power LED should be lit. If other LEDs are illuminated, it may be an indication that one or more of the FPGAs are not installed or programmed properly.

Appendix D - V233 Test Procedure

The V233 is tested using the VME test chassis and the associated LabView test program.