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V132 Gauss Time Line Generator Module Specification

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1. Theory of Operation

1.1 Functional Description

The Gauss Time Line Generator (V132 Module) is an event code generator module, which generates event codes at scheduled magnetic fields (as determined by the up/down gauss clock). The module takes the up gauss clock (pulses when magnetic field increases) and down gauss clock (pulses when magnetic field decreases), searches its users' schedule tables for a matched magnetic field value, and generates event codes at the matched field. The event codes are encoded and distributed throughout the accelerator complex via fiber optic links. To correct for the fact that the magnetic field may not be zero at the start of a cycle, a calibration value is loaded as the start magnetic field.

V132 module has an event link receiver and decoder circuit to decode the supercycle event codes from the Super-cycle generator (V130 module). These supercycle event codes are signals to various accelerator equipment systems to prepare for or start different activities. V132 module decodes and uses the following supercycle events: user code for PPM user change, prepulse code for updating the user table, T0 code for starting of an accelerator cycle, and group end code for the end of an accelerator cycles group.

V132 module has VME interface to communicate with the control software. It will allow software to setup user tables, read/write various status/command registers, and interrupt software for abnormal status.

V132 module is designed to work for both AGS and Booster accelerators. ASG and Booster have different gauss clock: one gauss clock equals to 0.05 Gauss for AGS and 0.1 Gauss for Booster. Thus the 24bit magnetic field value will span a field from 0-838 Kilogauss for AGS or 0-1.67 Mega-Gauss for Booster.

1.2 User tables

V132 module is a PPM user device and supports up to eight users. Each user has two user tables: active table for V132 to use for its searching; inactive table for software to update table contents. Each user table has 8K entries and each entry has 32bit data (24 bit for magnetic field value and 8 bit for event code value).

The 16 user tables are all saved on on-board user table SRAM. Software can update any of the tables and mark them one active and one inactive for each user. The user table to be used will depend on the user event received by V132. V132 module loads to the content addressable memory (see 1.3) and to the event code SRAM content from the user table SRAM when prepulse event happens. This loading procedure finishes before the cycle start (T0) event. From T0 event, V132 uses a new table for the searching and event code SRAM uses a new table for output event code. During this whole process, V132 module doesn't stop searching and generating event. It uses double buffer to do the searching and loading new table in parallel.

1.3 Searching using content address memory (CAM)

To quickly search through the 8K-entry table for a matched magnetic field value, V132 uses content addressable memory (CAM). CAM is a special type of memory used in certain very high speed searching applications. Unlike standard memory (random access memory or RAM) in which the user supplies a memory address and the RAM returns the data word stored at that address, a CAM is designed such that the user supplies a data word and the CAM searches its entire memory to see if that data word is stored anywhere in it. If the data word is found, the CAM returns a list of one or more storage addresses where the word was found. Because a CAM is designed to search its entire memory in a single operation, it is much faster than RAM in virtually all search applications. A typical application of CAM is in the design of communication router, which can quickly search through its routing table data to find a routing port for each IP packet and can also updating its routing table rapidly.

In V132 design, we use the CAM in the similar way as a router. The CAM is used in combination with a low-cost SRAM. Each 32bit user entry is saved at the same address location in CAM and SRAM: the 24bit magnetic field in CAM and 8bit event code in SRAM. When magnetic field changes, V132 control the CAM's searching port to search through the user table for a matched filed. Once a matched filed entry is found, CAM output the matched address that

drives the SRAM to output a event code. In the meantime, any user table change will cause V132 to update the CAM table through its maintenance port.

1.4 Eventlink

V132 generates Gauss event codes and output the code in parallel to a special P2 backplane. These parallel data are decoded by V197, V101 and encoded by V100. The encoded codes are transmitted using a serial modified Manchester code (bi-phase-mark). Each event code frame has one start bit, 8bit event code, one parity bit and two stop bits. The transmission rate is 10 M Bits/sec, and 1.2 usec are required to transmit an event code. The eventlink contains a continuous bi-phase-mark "ones' transmission during idle periods.

V132 module can also be setup to directly drive V100 encode module. The on-board jumpers will allow user to drive V197 or V100 module.

2. Hardware Description

2.1 Block diagram

The block diagram of V132 module is shown in Fig.1.

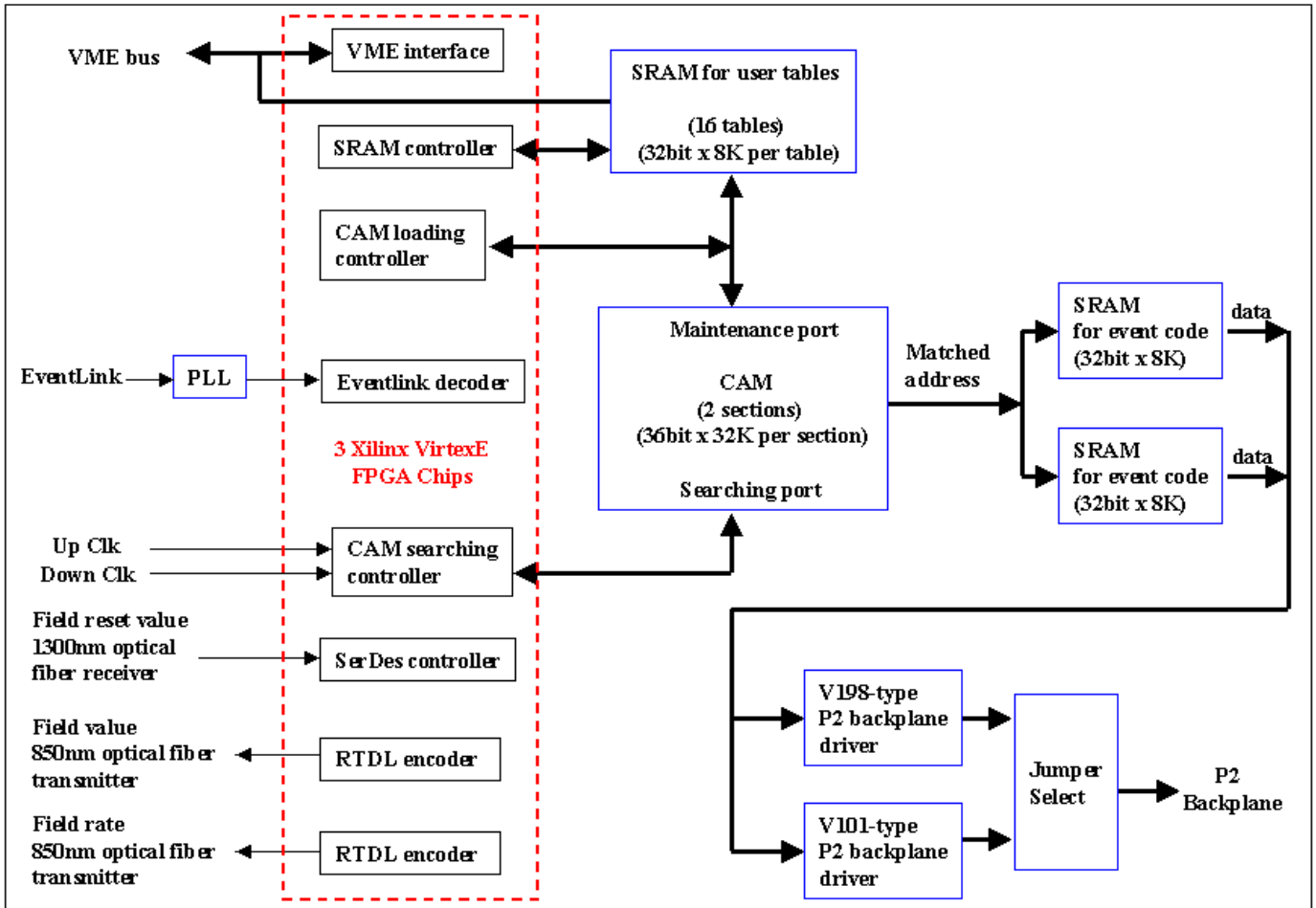

Figure 1. Block Diagram of V132 Module

2.2 Sub-block description

2.2.1 VME interface

VME interface handles the data transfer and interrupt cycle between V132 module and VME bus. It supports D8/D16 data mode and 39/3D address mode. The VME accessible data includes VME ID (a 64 byte embedded ROM for the module ID), 42 16bits registers for various status and command data, 512K byte user tables saved in SRAM, and embedded 3K byte RAM data for gauss field history read back.

There are 3 situations for V132 module to initiate a interrupt cycle: change of event link, change of field reset value fiber optical link and CAM loading control fail. Interrupt service route in software will read the status register and report these changes.

2.2.2 SRAM controller

SRAM controller is to control the normal read/write operation of the SRAM. It supports one byte and two bytes data transfer. The write operation is to write the data to SRAM through VME bus. The read operation can be read data to VME bus or read data to CAM for its loading operation. The address bus and data bus are shared between these operations through multiplexer.

2.2.3 CAM loading controller

CAM loading controller is to control the initialize the CAM and to load the gauss count data from user table SRAM to CAM through its maintenance port. It also needs to load the event code data from user table SRAM to event code SRAM.

To initialize the CAM, the controller needs to load several configuration registers for CAM's operation mode. To load the gauss count data, the controller needs to read the user table SRAM data and perform a write entry operation to the CAM. After finish the whole table writing operation, the controller read back both the CAM and user table SRAM data, compare each entry to confirm the correctness of the loading operation. During loading gauss count data to CAM, the controller also loads event code data to the event code SRAM. For each entry in user table, which consist of 24bit gauss count and 8bit event code, the controller load its gauss count and event code in the same address location in CAM and event code SRAM respectively. The whole loading operation is a fair complicated and is controller by several finite state machines.

2.2.4 CAM searching controller

The functions of CAM searching controller are to monitor the up and down gauss clock, calculate the magnetic field value, initiate a searching operation upon the change of magnetic field, and check the searching result if there is the magnetic field matches one entry in the CAM table. Several finite state machines are used to control the whole searching procedure.

2.2.5 Event link decoder

To decode event codes from event link, V132 module first decodes the clock and data from the serial event link stream using a phase lock loop circuit. Once the clock and data are separated, the event link decoder decodes the start, data, parity and stop bits. By compare the data with V132's registers, the decoder sends signals to other submodule to indicate the receipt of V132-related events such as USER, Prepule, T0 and Group End event.

2.2.6 SerDes controller (Gauss calibration circuit)

Field reset value (FRV) is delivered to V132 through a 1300nm multimode optical fiber. The transmitter uses transparent asynchronous xmitter –receiver interface (TAXI) chips. The data is encoded with 0-bit 5B/6B algorithm. V132 module uses a TAXI-compatible receiver chip to deserilize the data. The SerDes controller is to control the receiver chip and reconstruct the FRV value.

2.3 Memory map

The following table shows the VME memory map for V132 module.

Table 1: Memory map of V132 module (64K VME space. 39/3D address mode. D8/D16 data mode)

Resister or Memory	Function	Size (byte)	Address (offset to base address) and FEC access mode
VME ID	V132 Module ID and Serial Number	64	0x00 – 0x7F (Rd)
Command Register	Bit map: Bit[15]: FEC_ready: 1: FEC has loaded the necessary registers and is ready. 0: FEC is not ready. Bit [14:12]: Reserved Bit[11]: Set gauss field history record clock speed 1: Fast speed (1.6384 ms per point). 0: Slow speed (13.1072ms per point). Bit[10]: Reset timing counter. 1: Reset the counter to zero. 0: Not reset. Bit [9]: Reset down clock counter 1: Reset the counter to zero. 0: Not reset. Bit [8]: Reset up clock counter 1: Reset the counter to zero. 0: Not reset. Bit[7]: Set FRV mode 1: Auto load FRV value at the FRV start pulse. 0: Load FRV maual value at T0 event. Bit [6:5]: Reserved. Bit [4]: Eventlink_code_reg_loaded 1: USER, PP, T0 and GEND code registers are valid. 0: Not valid. Bit [3:0]: VME access table index When FEC needs to access user table SRAM memory, use these bits to select one of the 16 tables for its operation. 0x0 for table 1. 0xF for table 16.	2	0x80 – 0x81 (Wr/Rd)
Table valid register	• 16 bit for 16 user table's validation status. 1=valid 0=invalid. • Each user has two tables (A and B). They are mapped as the following: Bit[15:0] = {8B 8A 7B 7A 6B 6A 5B 5A 4B 4A 3B 3A 2B 2A 1B 1A}	2	0x82 – 0z83 (Wr/Rd)
Table touched register	• 16 bit for 16 user table's implementation status. 1=Not loaded and used. 0=loaded and used. • Each user has two tables (A and B). They are mapped as the following: Bit[15:0] = {8B 8A 7B 7A 6B 6A 5B 5A 4B 4A 3B 3A 2B 2A 1B 1A}	2	0x84 – 0x85 (Rd)
Interrupt ID level register	Bit[15:11]: reserved. Bit[10:8]: Interrupt level. Bit[7:0]: Interrupt state/ID.	2	0x86 – 0x87 (Wr/Rd)
U1 U2 code register	Bit[15:8]: event code for user 1. Bit[7:0]: event code for user 2. (for AGS: 0x1516; for Booster: 0x0B0C)	2	0x88 – 0x89 (Wr/Rd)
U3 U4 code register	Bit[15:8]: event code for user 3. Bit[7:0]: event code for user 4. (for AGS: 0x1718; for Booster: 0x0D0E)	2	0x8A – 0x8B (Wr/Rd)
U5 U6 code register	Bit[15:8]: event code for user 5. Bit[7:0]: event code for user 6.	2	0x8C – 0x8D (Wr/Rd)
U7 U8 code register	Bit[15:8]: event code for user 7. Bit[7:0]: event code for user 8.	2	0x8E – 0x8F (Wr/Rd)
PP T0 code register	Bit[15:8]: pre-pulse event code. Bit[7:0]: event code for cycle start T0. (for AGS: 0x1D14; for Booster: 0x130A)	2	0x90 – 0x91 (Wr/Rd)
Group End code register	Bit[15:8]: 0x00. Bit[7:0]: group end code.. (for AGS: 0x001C; for Booster: 0x0012)	2	0x92 – 0x93(Wr/Rd)

Memory map of V132 module (con't)

Status register	Bit[15]: CAM initialization done. 1= CAM is initialized. 0=CAM initialization fails. Bit[14]: CAM is searching. 1= CAM in searching mode. 0=CAM stop searching due to load error. Bit[13]: Load success 1= Load success in the last loading attempt. 0= Load fail due to bad table. Bit[12]: Table valid true. Falling edge causes interrupt. 1= Table valid for the user. 0= No valid table for the user Bit[11]: Bad table. Rising edge causes interrupt. 1= Find bad table (no ending mark) during loading. 0=Table good. Bit[10]: Eventlink PLL locked. Change value cause interrupt. 1 = Locked. 0= Unlocked. Bit[9]: FRV link good. Change value causes interrupt. 1= FRV link good. 0= FRV link fail. Bit[8]: V101_overflow (when V132 used V101-type driver). Rising edge cause interrupt. FEC read status register will clear this bit. 1= Overflow. 0= No overflow. Bit[7:4]: Inactive table index. Table in the inactive(non-searching) section of CAM. Bit[3:0]: Active table index. Table in the active(searching) section of CAM	2	0x94 – 0x95 (Rd)
Gauss count high register	Gauss count's high word.	2	0x96 – 0x97 (Rd)
Gauss count low register	Gauss count's low word.	2	0x98 – 0x99 (Rd)
Gauss count high word for the most recent match	Gauss count's high word when V132 finds a match and generate event code most recently.	2	0x9A – 0x9B (Rd)
Gauss count low byte word and event code for the most recent match	Bit[15:8]: Gauss count's low byte word when V132 finds a match and generate event code most recently. Bit[7:0]: The event code V132 generated most recently.	2	0x9C – 0x9D (Rd)
Tables in previous group	4 user table index for the table used during the previous group. Bit[3:0] for the most recent one and so on.	2	0x9E – 0x9F (Rd)
Timing count high register	Timing count's high word. Timing count starts at cycle start and ends at group end. Each step is 25ns.	2	0xA0 – 0xA1 (Rd)
Timing count low register	Timing count's low word.	2	0xA2 – 0xA3 (Rd)
FRV auto high register	Auto FRV's high word. Auto FRV value is obtained from the FRV optical fiber link.	2	0xA4 – 0xA5 (Rd)
FRV auto low register	Auto FRV's low word. Auto FRV value is obtained from the FRV optical fiber link.	2	0xA6 – 0xA7 (Rd)
FRV manual high register for User 1	Manual FRV's high word for user 1.	2	0xA8 – 0xA9 (Wr/Rd)
FRV manual low register for User 1	Manual FRV's low word for user 1.	2	0xAA– 0xAB (Wr/Rd)
FRV manual high register for User 2	Manual FRV's high word for user 2.	2	0xAC– 0xAD (Wr/Rd)
FRV manual low register for User 2	Manual FRV's low word for user 2.	2	0xAE– 0xAF (Wr/Rd)
FRV manual high register for User 3	Manual FRV's high word for user 3.	2	0xB0– 0xB1 (Wr/Rd)
FRV manual low register for User 3	Manual FRV's low word for user 3.	2	0xB2– 0xB3 (Wr/Rd)
FRV manual high register for User 4	Manual FRV's high word for user 4.	2	0xB4– 0xB5 (Wr/Rd)
FRV manual low register for User 4	Manual FRV's low word for user 4.	2	0xB6– 0xB7 (Wr/Rd)

Memory map of V132 module (con't)

FRV manual high register for User 5	Manual FRV's high word for user 5.	2	0xB8– 0xB9 (Wr/Rd)
FRV manual low register for User 5	Manual FRV's low word for user 5.	2	0xBA– 0xBB (Wr/Rd)
FRV manual high register for User 6	Manual FRV's high word for user 6.	2	0xBC– 0xBD (Wr/Rd)
FRV manual low register for User 6	Manual FRV's low word for user 6.	2	0xBE– 0xBF (Wr/Rd)
FRV manual high register for User 7	Manual FRV's high word for user 7.	2	0xC0– 0xC1 (Wr/Rd)
FRV manual low register for User 7	Manual FRV's low word for user 7.	2	0xC2– 0xC3 (Wr/Rd)
FRV manual high register for User 8	Manual FRV's high word for user 8.	2	0xC4– 0xC5 (Wr/Rd)
FRV manual low register for User 8	Manual FRV's low word for user 8.	2	0xC6– 0xC7 (Wr/Rd)
Up clk count high register	Up clock count's high word. Reset at T0 and increased by 1 at each up clock.	2	0xC8– 0xC9 (Rd)
Up clk count low register	Up clock count's low word.	2	0xCA– 0xCB(/Rd)
Down clk count high register	Down clock count's high word. Reset at T0 and increased by 1 at each down clock.	2	0xCC– 0xCD (Rd)
Down clk count low register	Down clock count's low word.	2	0xCE– 0xCF (Rd)
Gauss field RAM point register	Bit[15]: Gauss field history record speed. 1: Fast speed (1.6384 ms per point). 0: Slow speed (13.1072ms per point). Bit[14:0]: Valid number of data point in the embedded Gauss field RAM. Maximum is 1023.	2	0xD0– 0xD1 (Rd)
Embedded Gauss field RAM	Record the magnetic field history in the previous group. Can record maximum 1024 points. Each data point is 24bit in the RAM and is mapped to 32bit in VME space with the upper one byte always equal to zero.	4K	Start address: 0x2000 End address: 0x3000
User table SRAM	Only one user table (32bit x 8K) is mapped into VME space. To access each of the 16 user tables, FEC needs to setup the table index, which is the last four bits of command register.	32K	Start address: 0x8000 End address: 0xFFFF

2.4 Hardware design/simulation/test issue

2.4.1 Hardware design and simulation issue

The FPGA design is done using Verilog HDL in Xilinx ISE6.1 design environment. The simulation is done using Mentor Graphics ModelSim 5.8. By using the simulation models provided by IC vendors, such as the CAM and SRAM simulation modules, the whole digital system of the V132 design is simulated together using ModelSim. Such a system simulation let us find any system integration error quickly and easily. It also allow us to simulate some of the complicated board functions.

The PC board design and layout is done using Altium's P-CAD PCB design software. The whole signals are routed on a 10-layer PC board.

2.4.2 Test issue

To test V132 module, a complete test procedure has been developed. Please refer the Test Procedure of V132 Module.

3. Control Software Description

The V132 module control software consists of VxWorks device driver and user interface. The software design is descried in separate document. It will be useful to show a simple timing diagram for some of the hardware and software tasks in Figure 2.

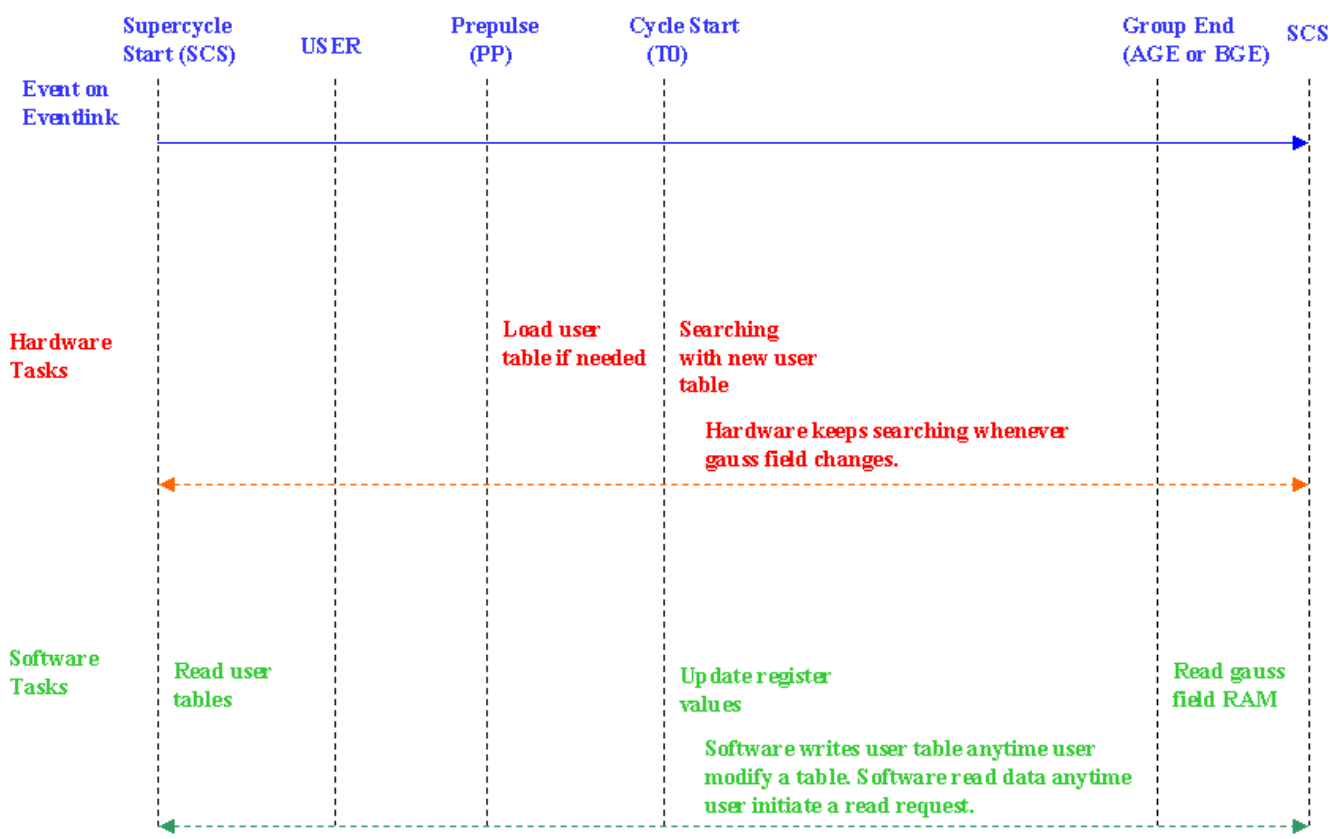

Figure 2. Primary timing diagram of hardware and software tasks