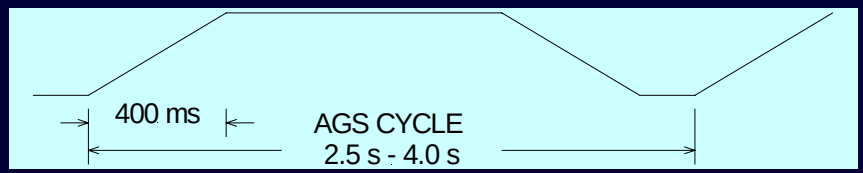
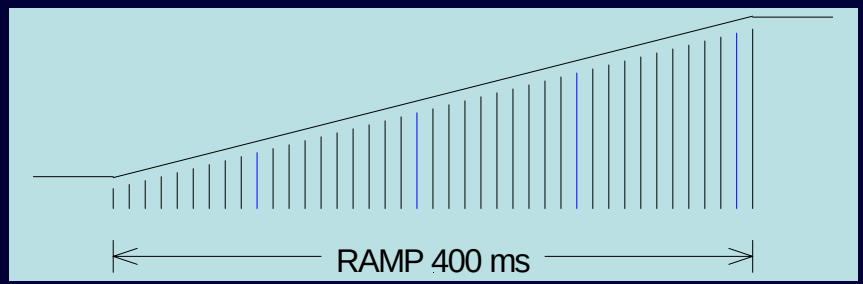
Polarized Proton Beam Weak Resonance Correction by Pulsed Quads

Arlene Zhang, Jon Sandberg

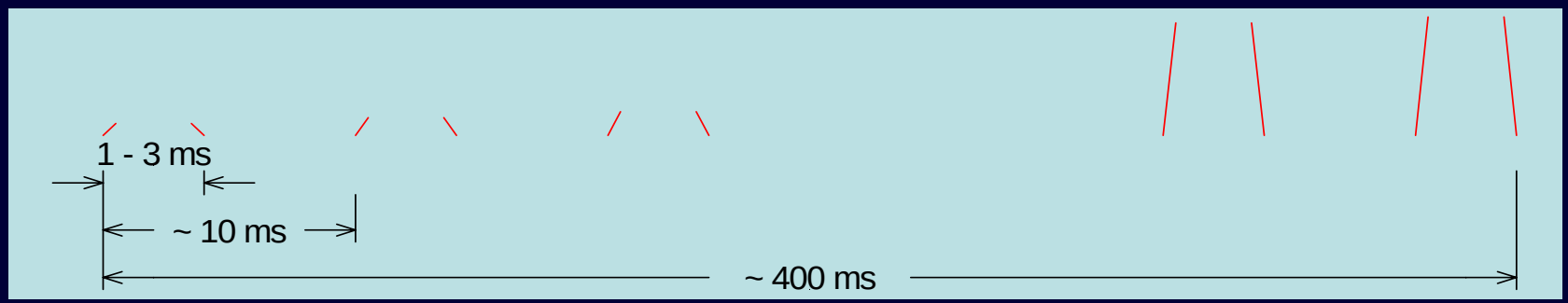
July 16, 2008

Main Specifications

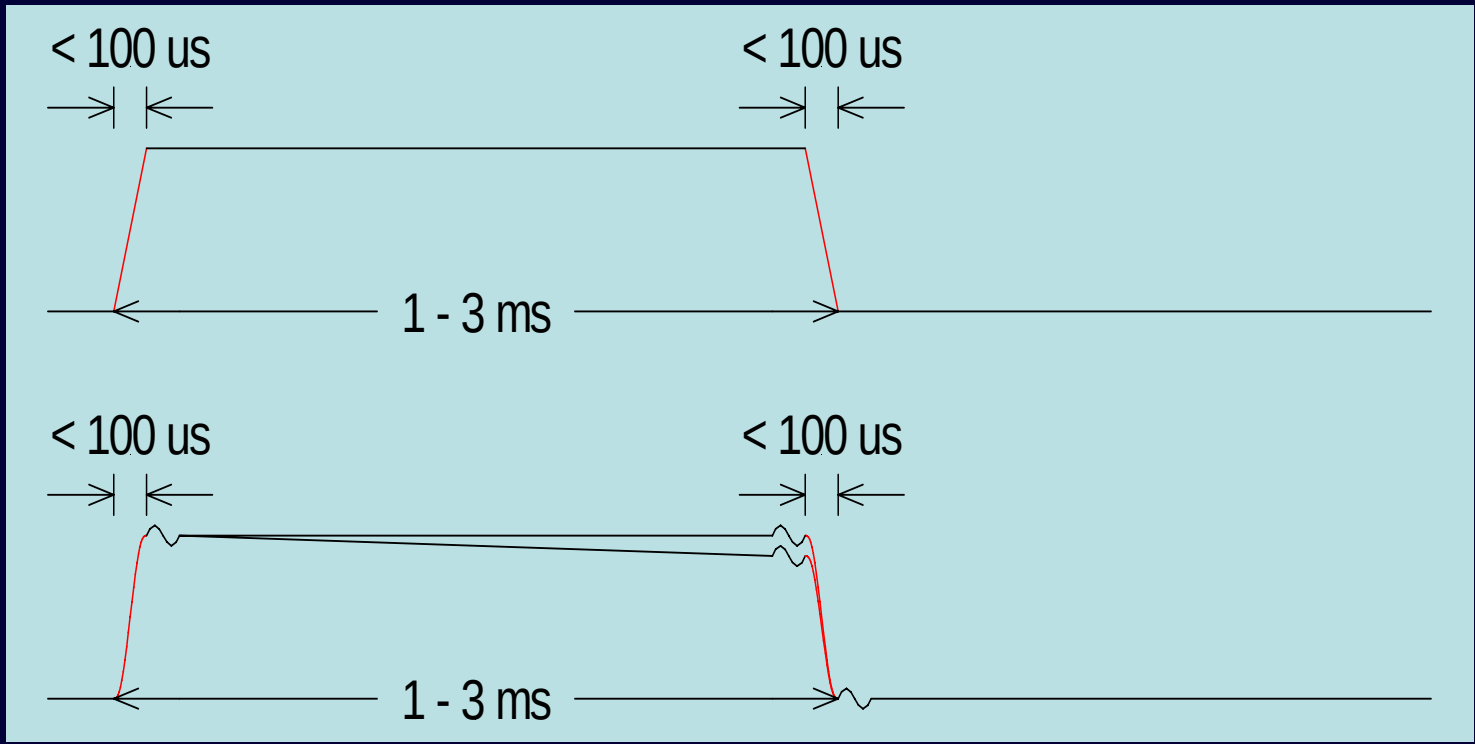




- 41 pairs of +/- tune jumps during 400 ms ramp
- AGS cycle 2.5 s to 4 s
- 4 quads in AGS D5, I5, J5, L5
- 240 A to 2400 A pulsed current



Pulse Waveform Specifications
Option 1 – Trapezoidal



RMS Current

- 240A to 2400A, 54A step
- 100 us rise or fall time
- 1ms flat top or decay time
- 400 ms AGS ramp time
  - RMS current (ramp) = 148.83 A
- Per AGS cycle 2.5s
  - RMS Current (AGS cycle) = 23.813 A
- Per AGS cycle 4.0s
  - RMS Current (AGS cycle) = 14.883 A

RMS Current

Pulse Length	1 ms	2 ms	3 ms
I_rms (Ramp)	148.3 A	284.1 A	419.4 A
I_rms (2.5s AGS cycle)	23.8 A	45.5 A	67.1 A
I_rms (4.0s AGS cycle)	14.9 A	28.4 A	41.9 A

Trapezoidal Pulse: Adjustable flat top

- ? the longer the flat top, the larger the capacitor bank, or the larger the flat top drop.
- ? Symmetric ???

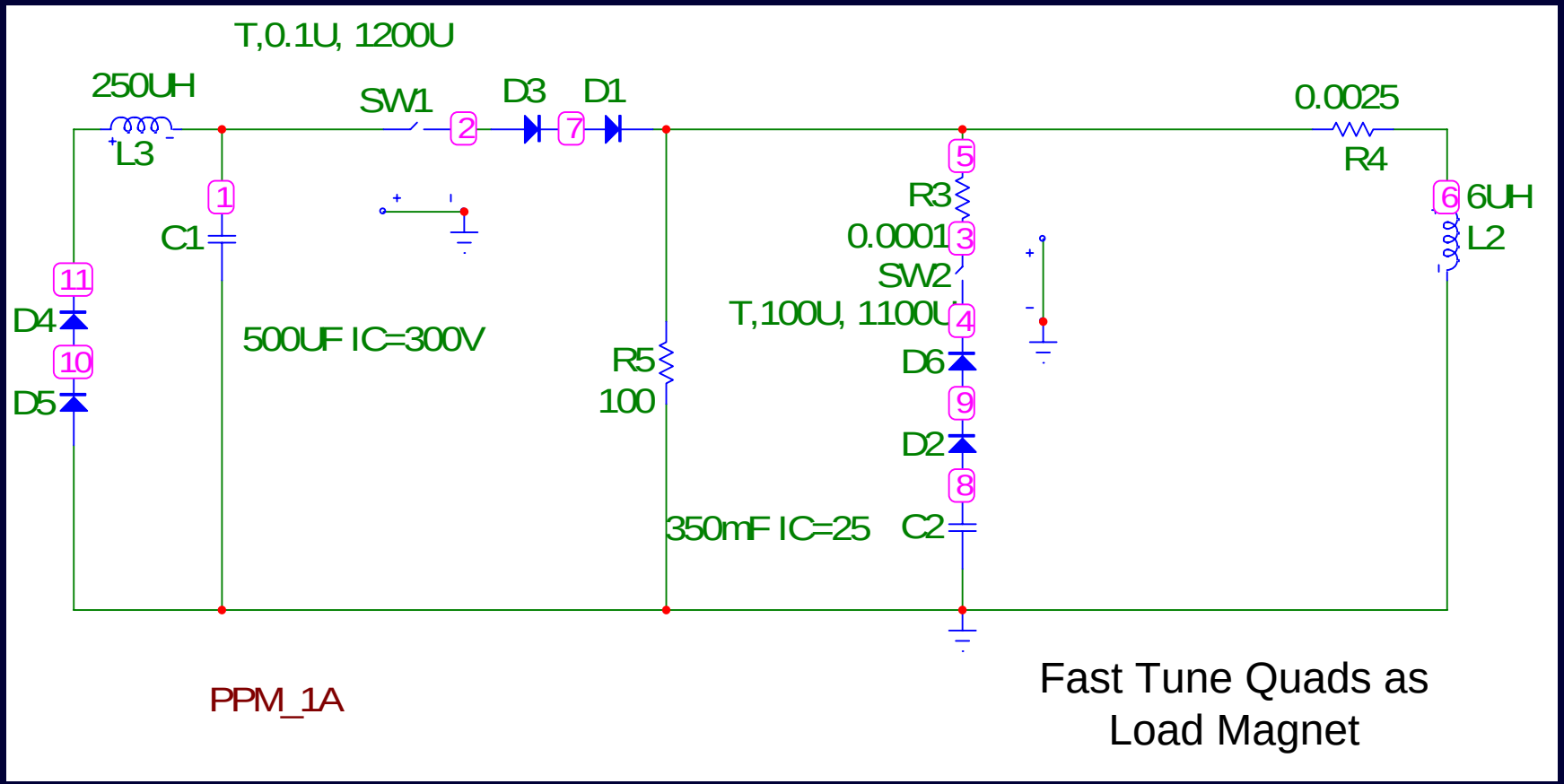
Bipolar Triangle Pulse: Adjustable quiet zone (or adjustable decay)

- ✓ Symmetric

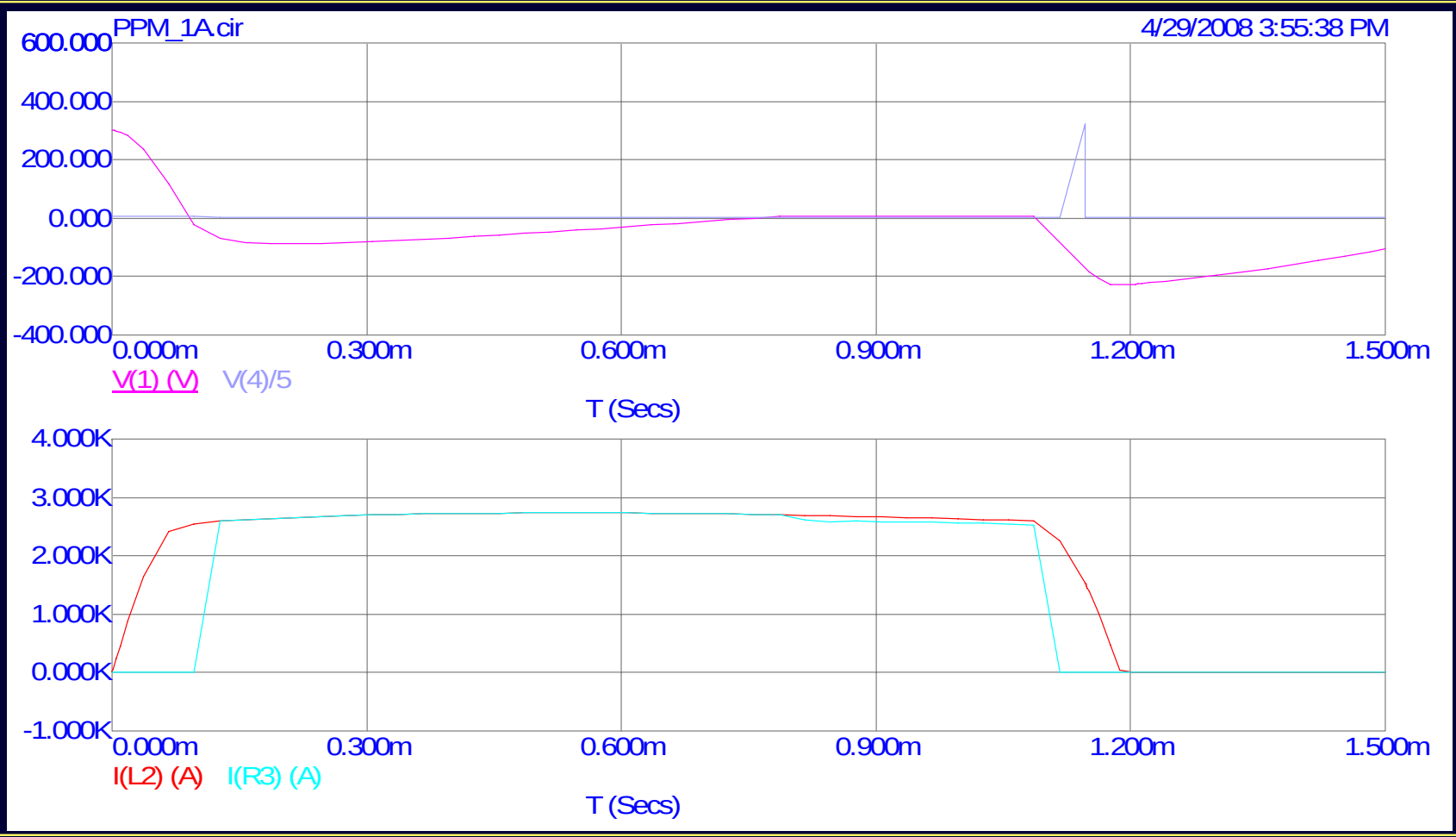
Key Issues

- Cable Inductance
- Pulse Symmetry
- Pulse Overshoot
- Pulse Undershoot
- Pulse Flat-top
- Circuit Resistance
- System Cooling

Woody's Suggested Circuit (inside tunnel without cable option)



Simulation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4/29/2008 3:55:38 PM
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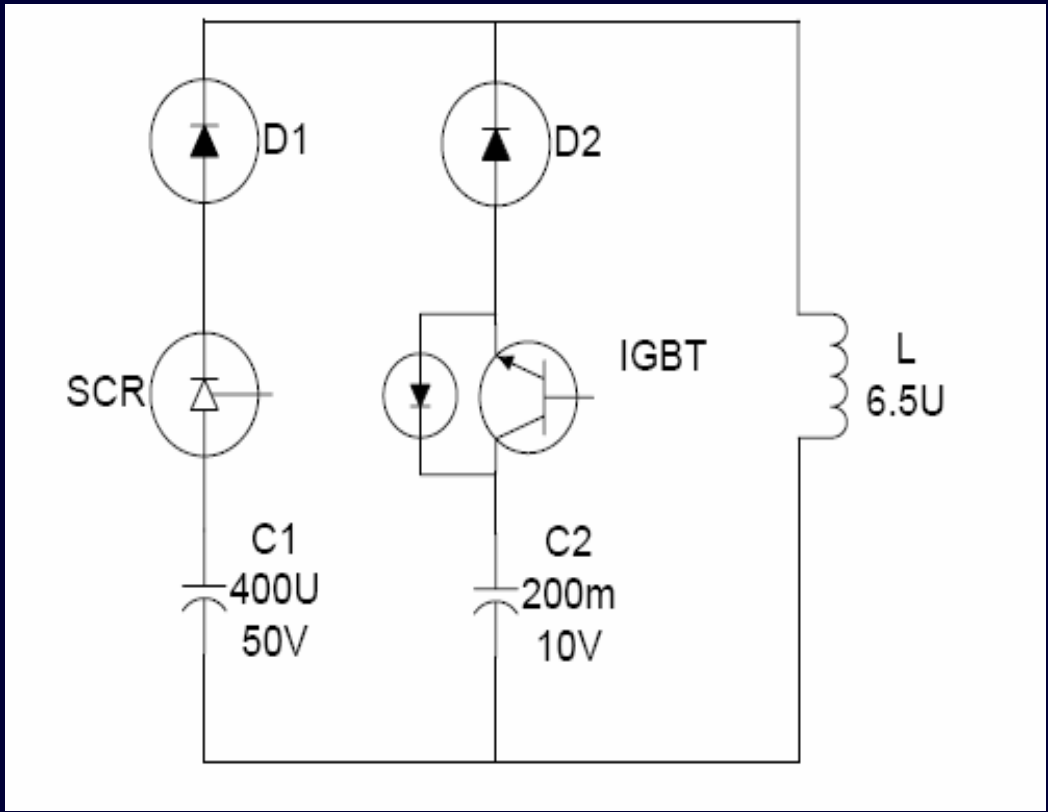
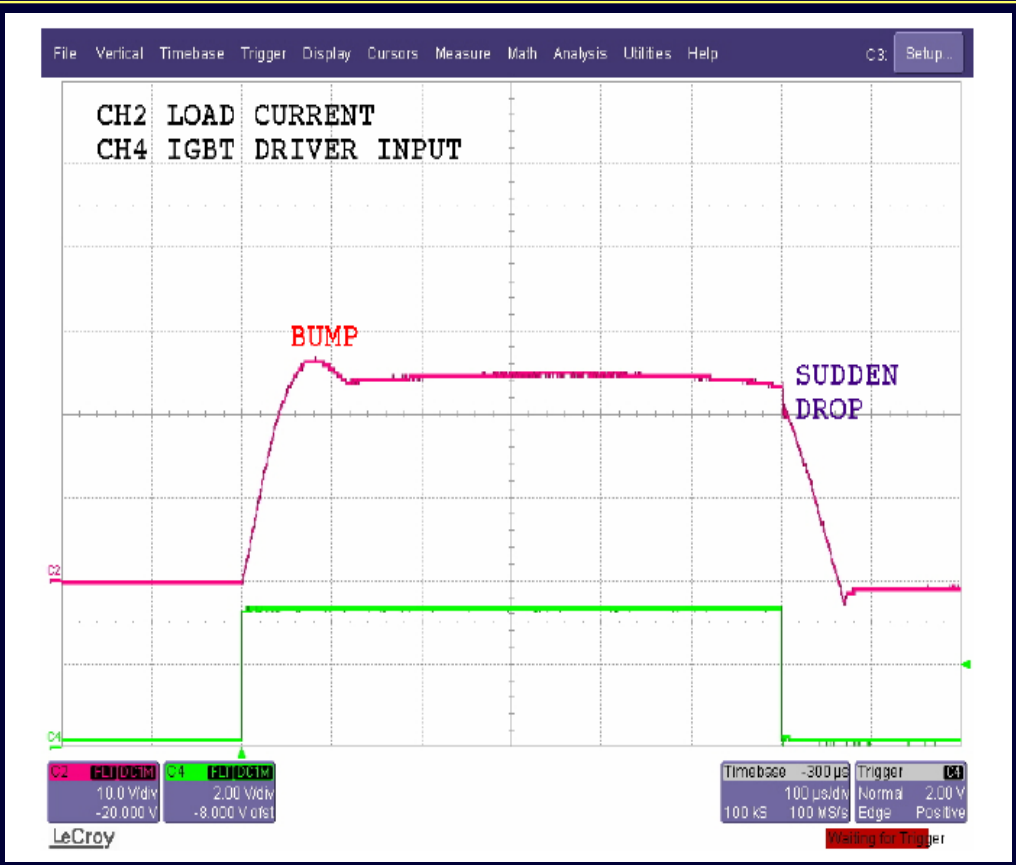
400.000
200.000
0.000
-200.000
-400.000
0.000m
0.300m
0.600m
0.900m
1.200m
1.500m
V(1) (V)
V(4)/5
T (Secs)
4.000K
3.000K
2.000K
1.000K
0.000K
-1.000K
0.000m
0.300m
0.600m
0.900m
1.200m
1.500m
I(L2) (A)
I(R3) (A)
T (Secs)

Test Circuit



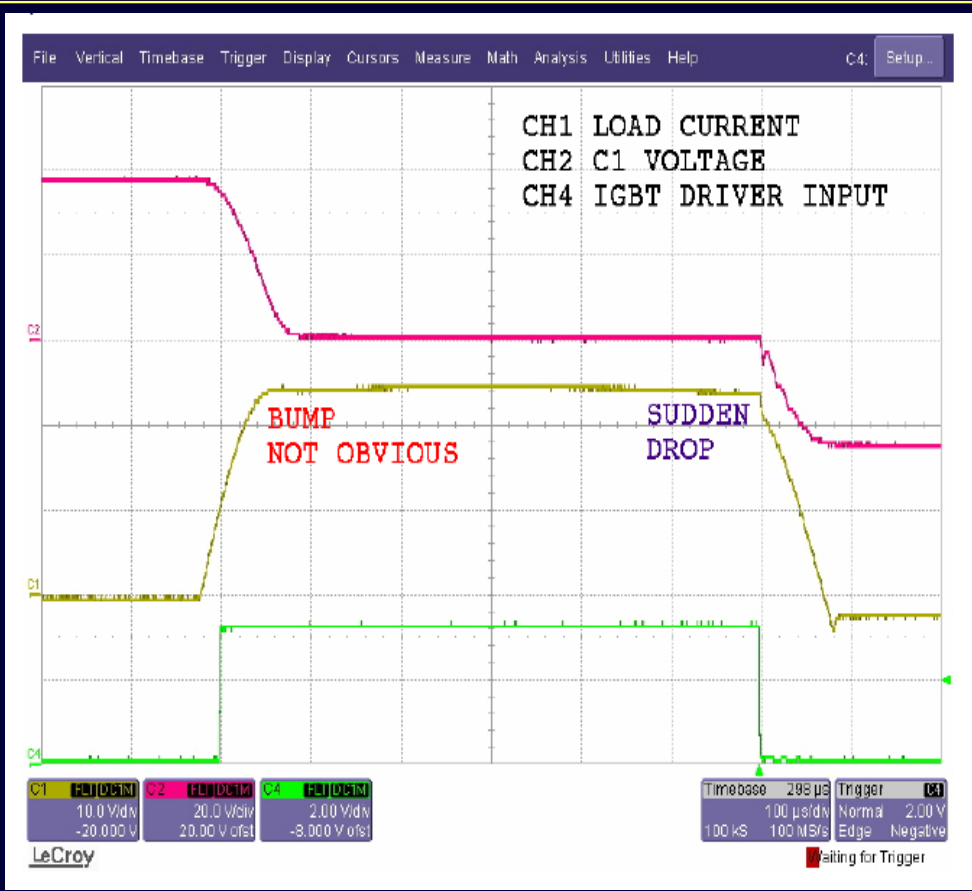
Yugang's test setup

Test Performance



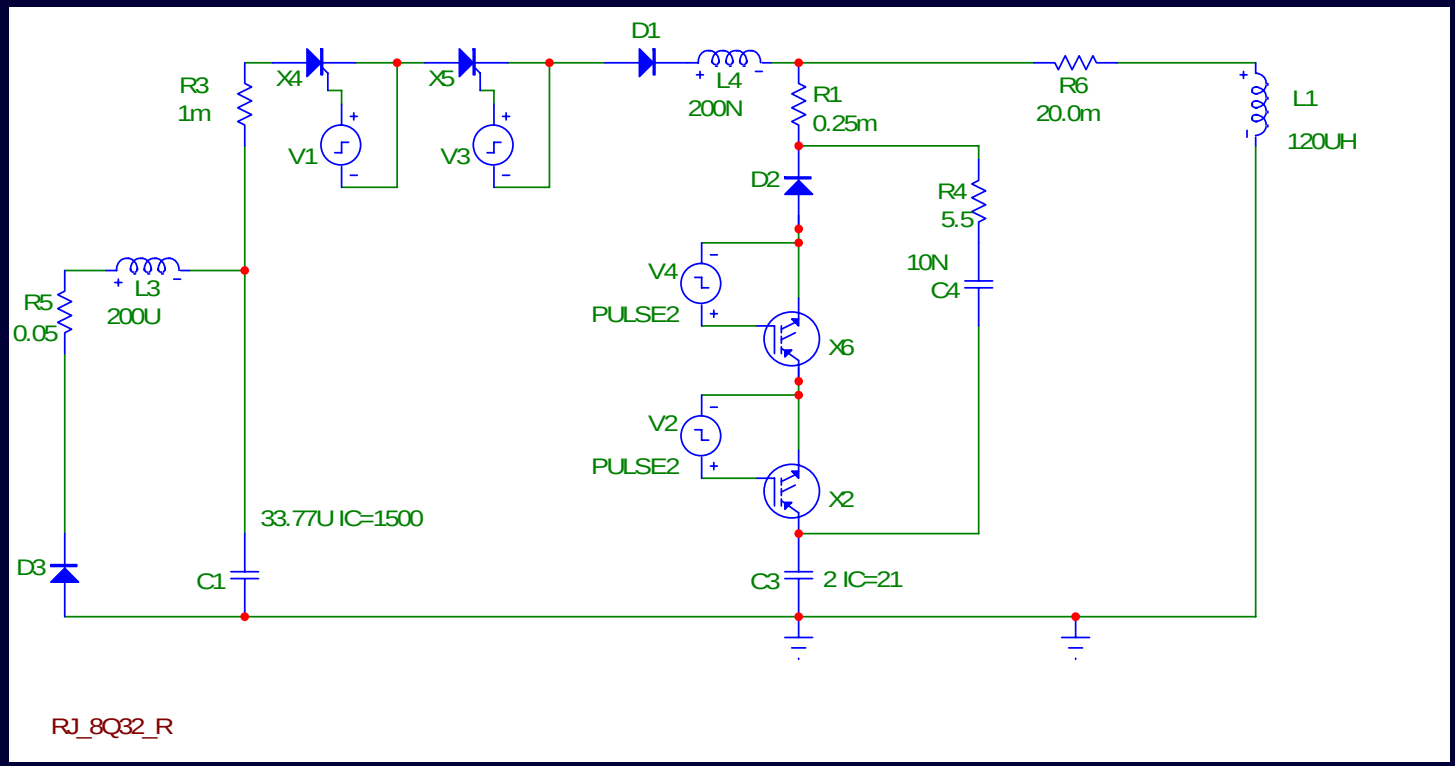
Provided by Yugang Tan

Test Performance



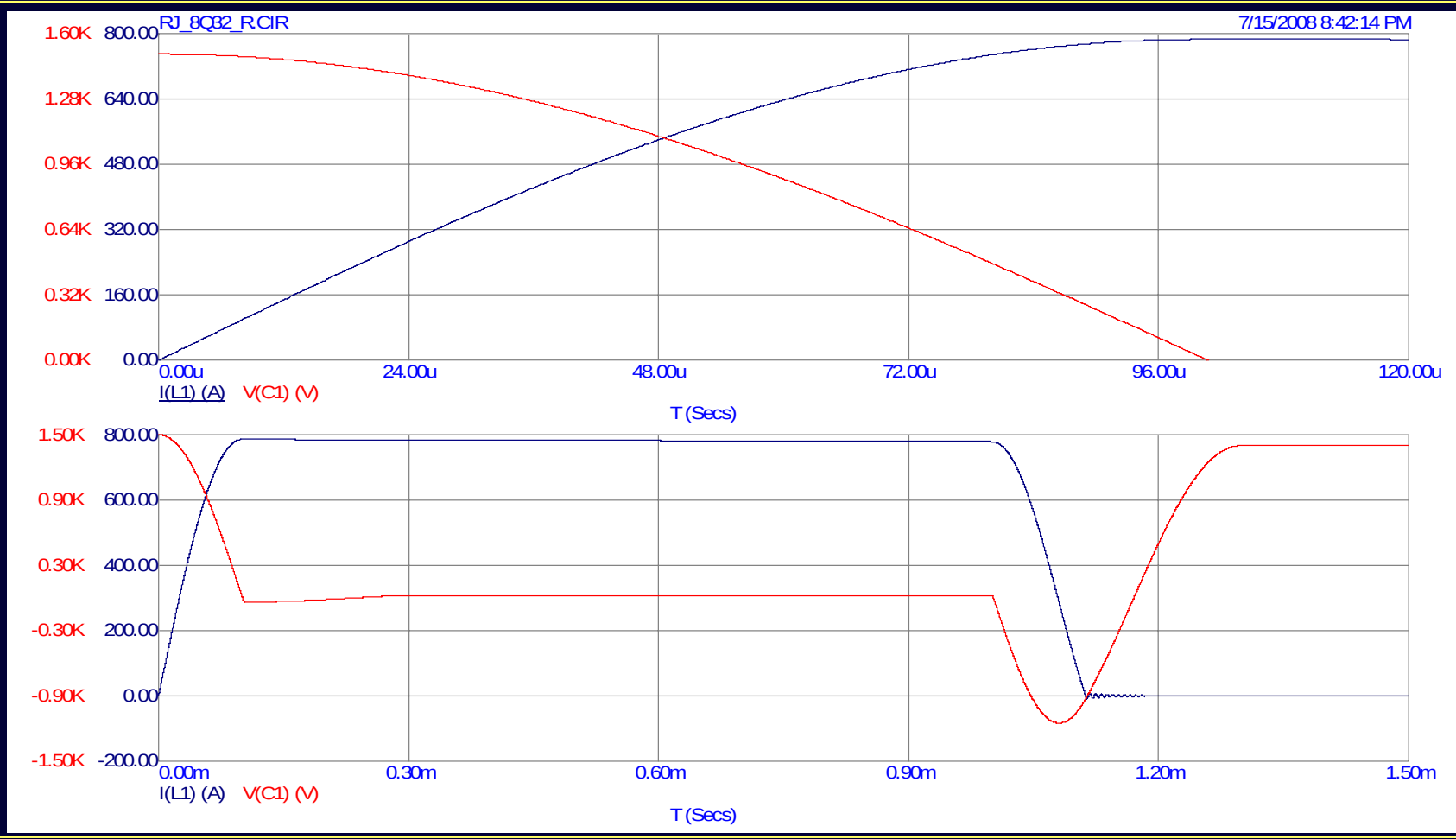
Provided by Yugang Tan

8Q32 with Quadruplex Cable



Estimation of cable & load inductance of 120 uH is by Jianlin Mi

Simulation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7/15/2008 8:42:14 PM
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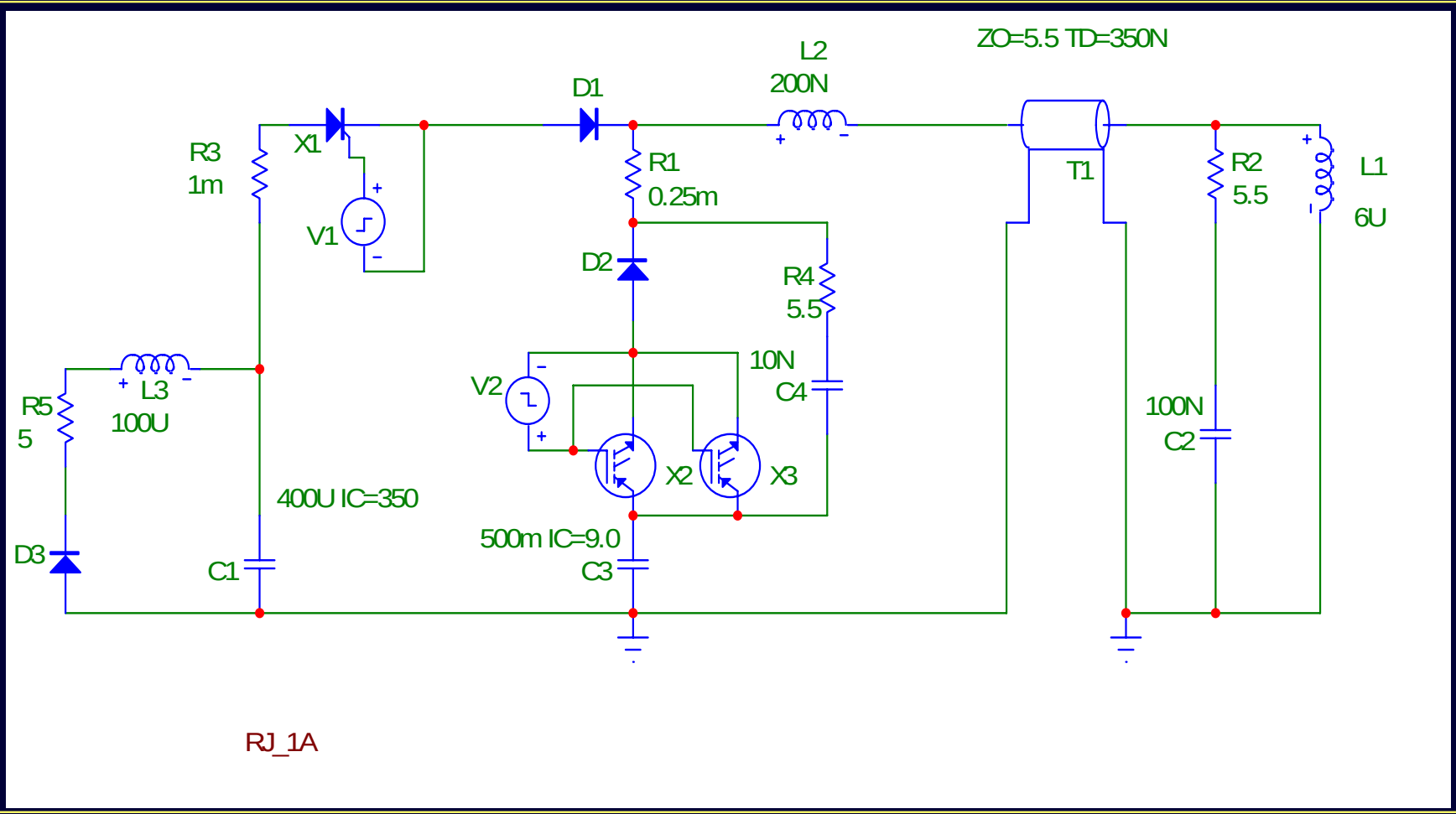
1.28K
0.96K
0.64K
0.32K
0.00K
800.00
640.00
480.00
320.00
160.00
0.00
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
1.50K
0.90K
0.30K
-0.30K
-0.90K
-1.50K
800.00
600.00
400.00
200.00
0.00
-200.00
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

Concerns

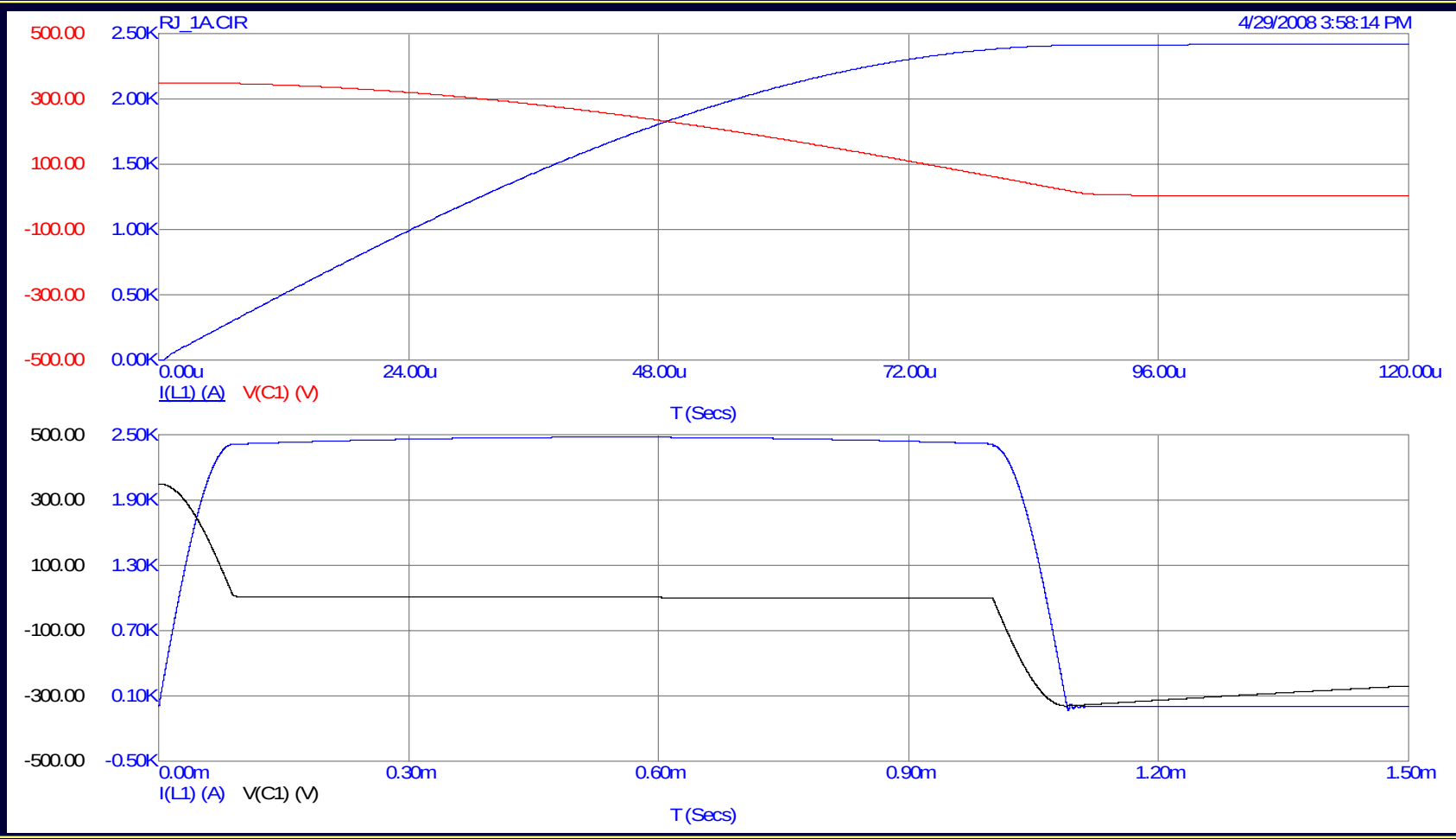
- High voltage 1500V
  - Voltage is higher than existing fast bump capacitor rating
- High energy storage
- Large cable inductance
- Inefficiency
- Component Selection

Proposed Schematic

(Fast Tune Quads with Coaxial Cable)



Simulation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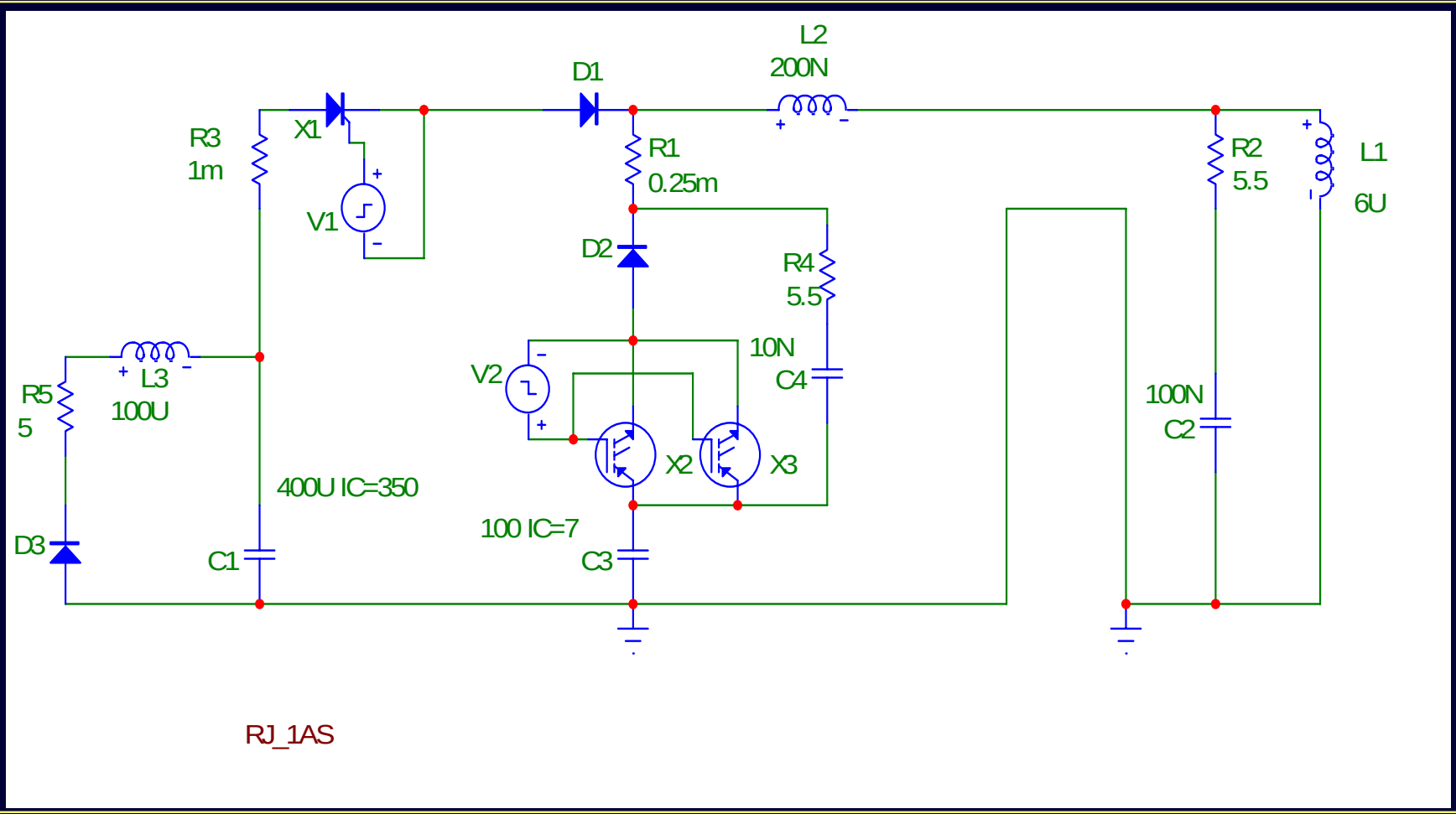
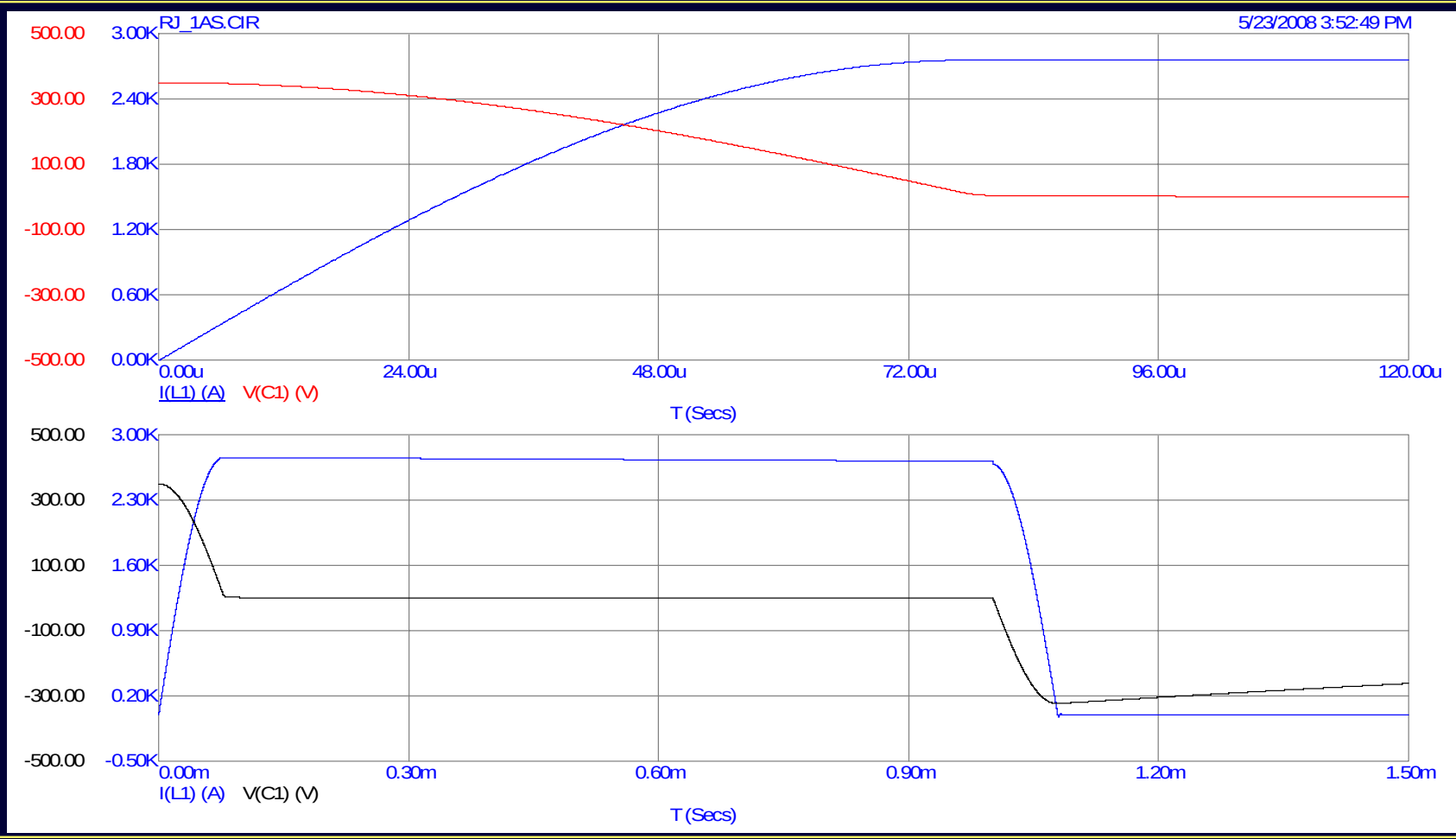
100.00
-100.00
-300.00
-500.00
2.50K
2.00K
1.50K
1.00K
0.50K
0.00K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

Proposed Test Schematic

(Fast Tune Quads inside tunnel directly connected)



Simulation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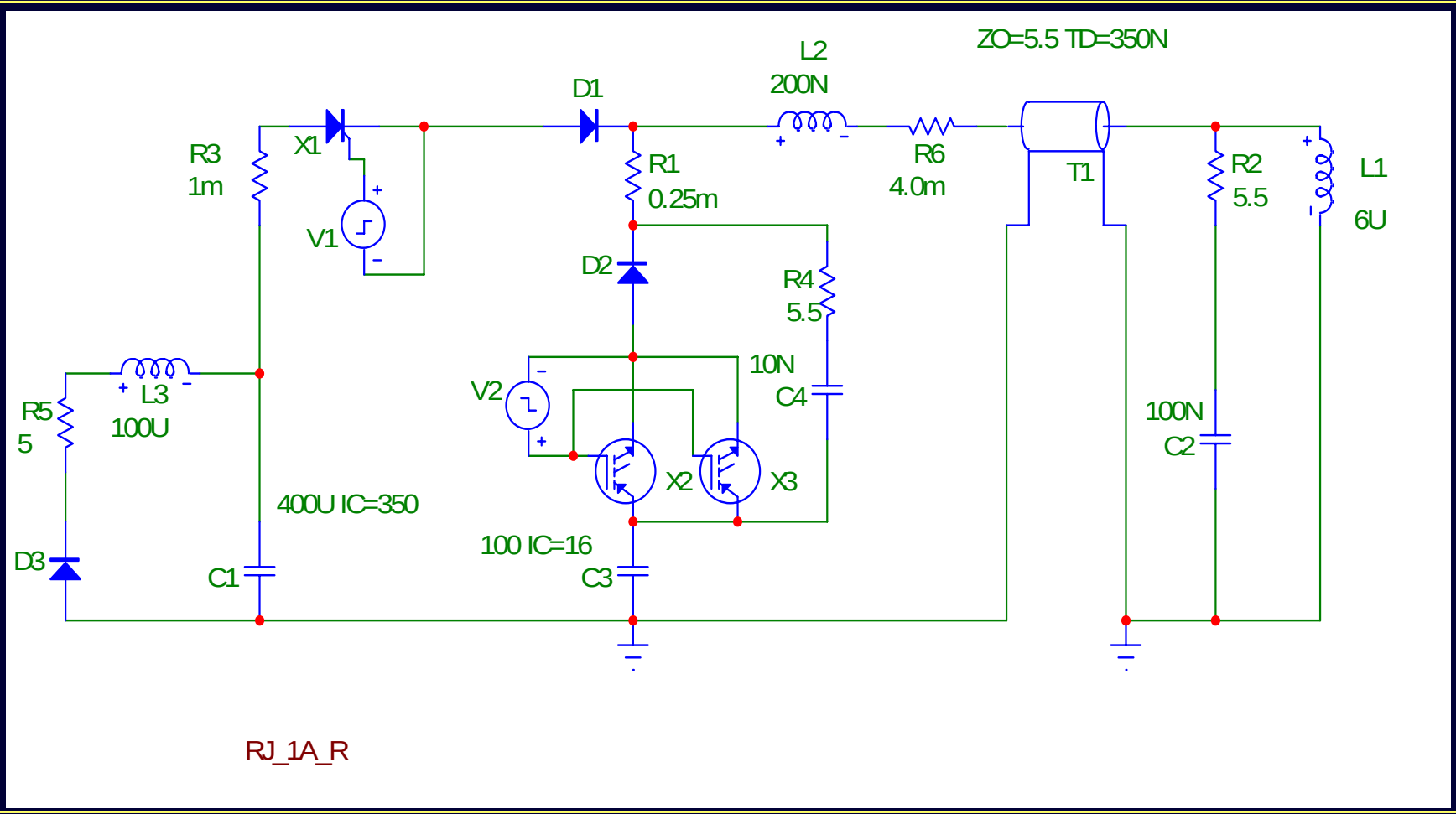
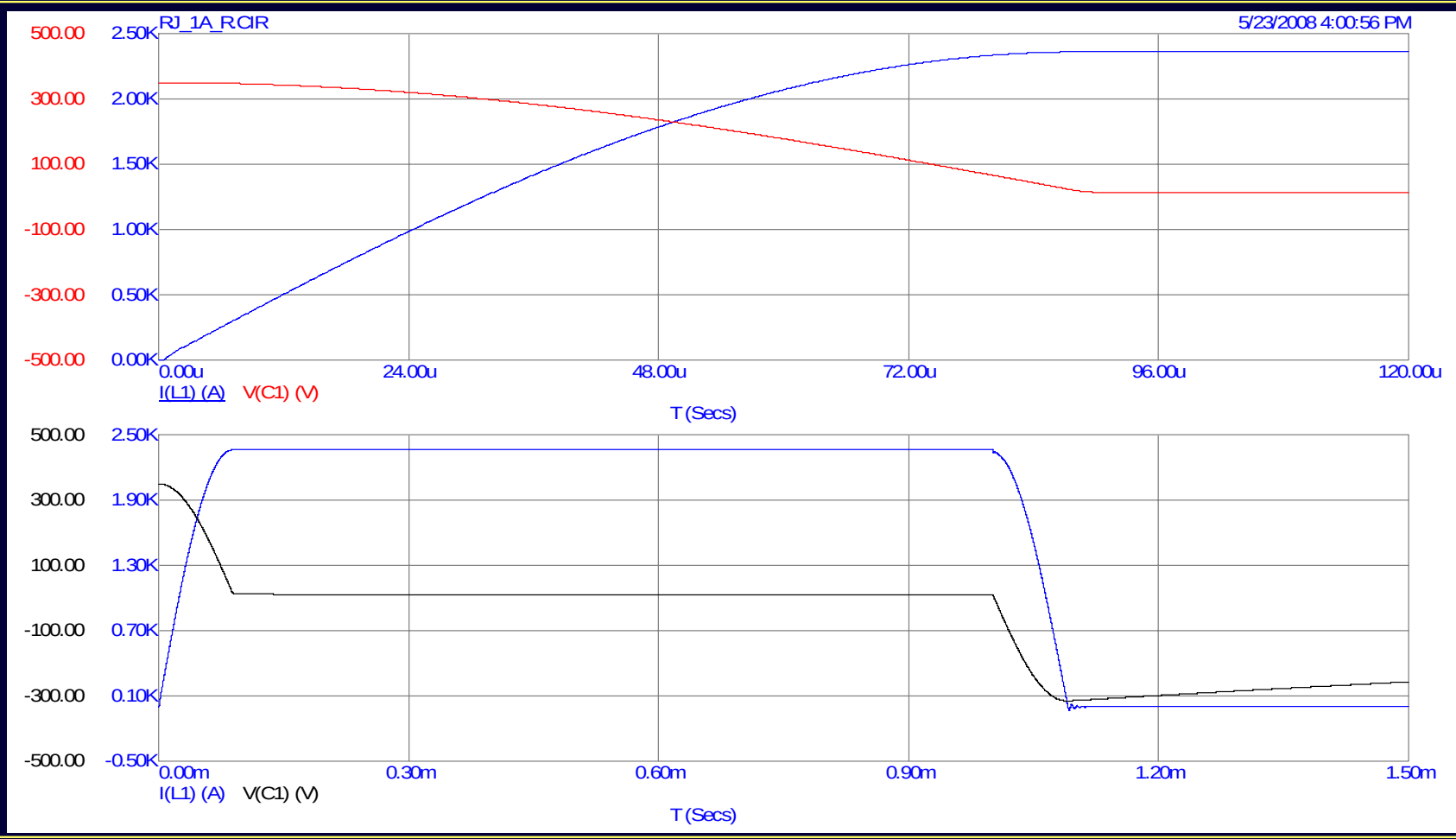
100.00
-100.00
-300.00
-500.00
3.00K
2.40K
1.80K
1.20K
0.60K
0.00K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
3.00K
2.30K
1.60K
0.90K
0.20K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

Resistance Effect



Simulation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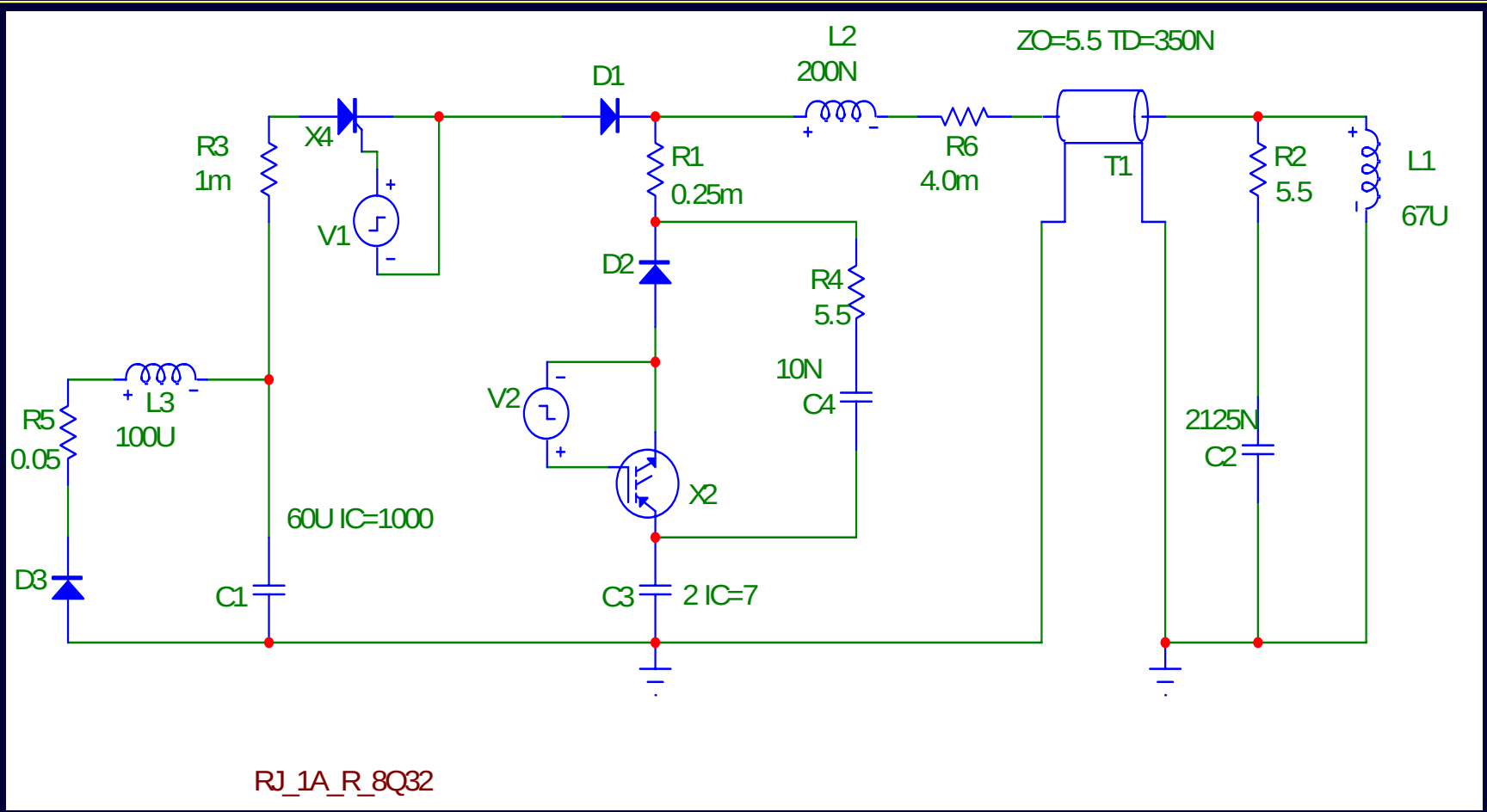
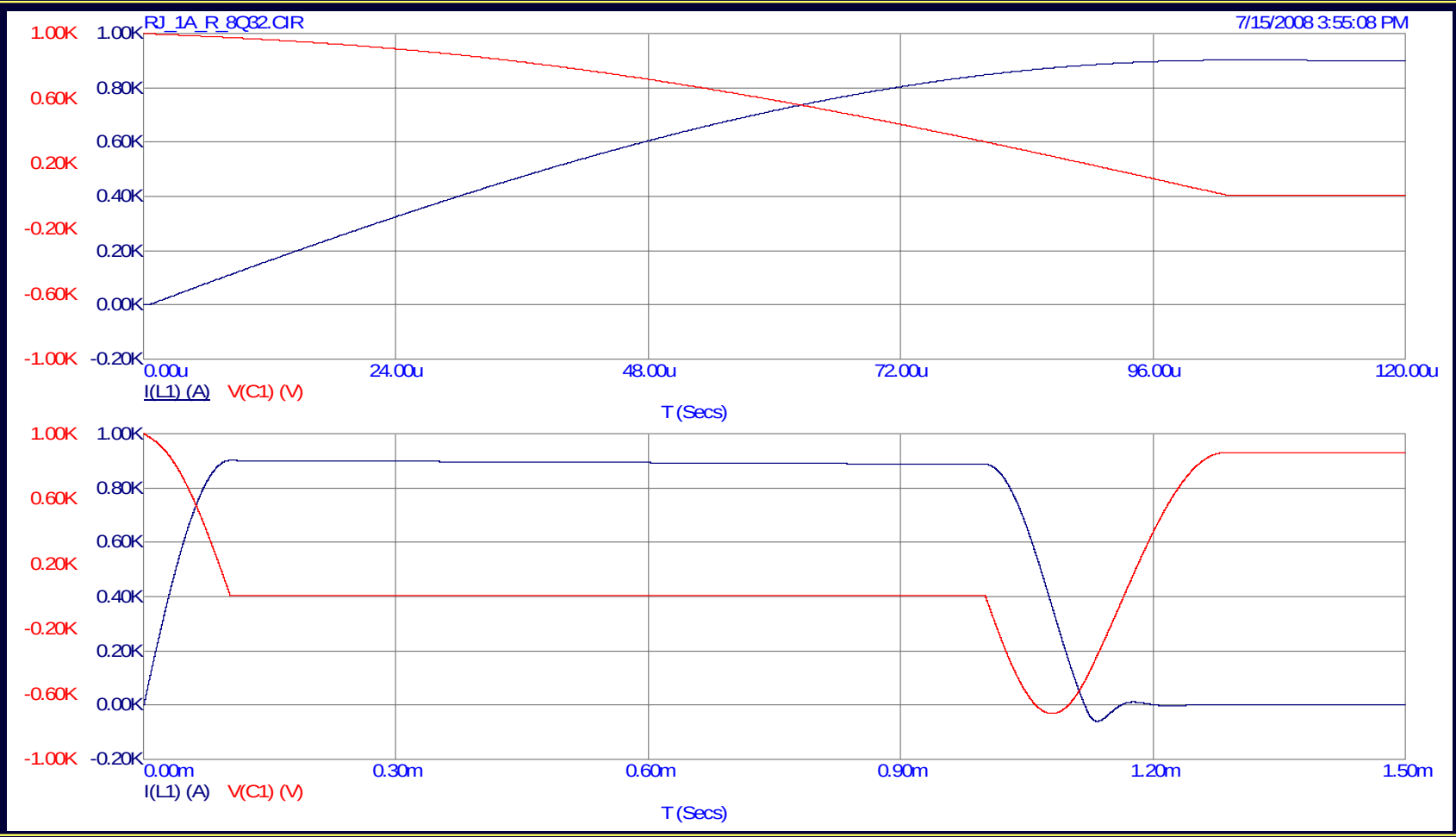
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
2.00K
1.50K
1.00K
0.50K
0.00K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

Proposed Schematic

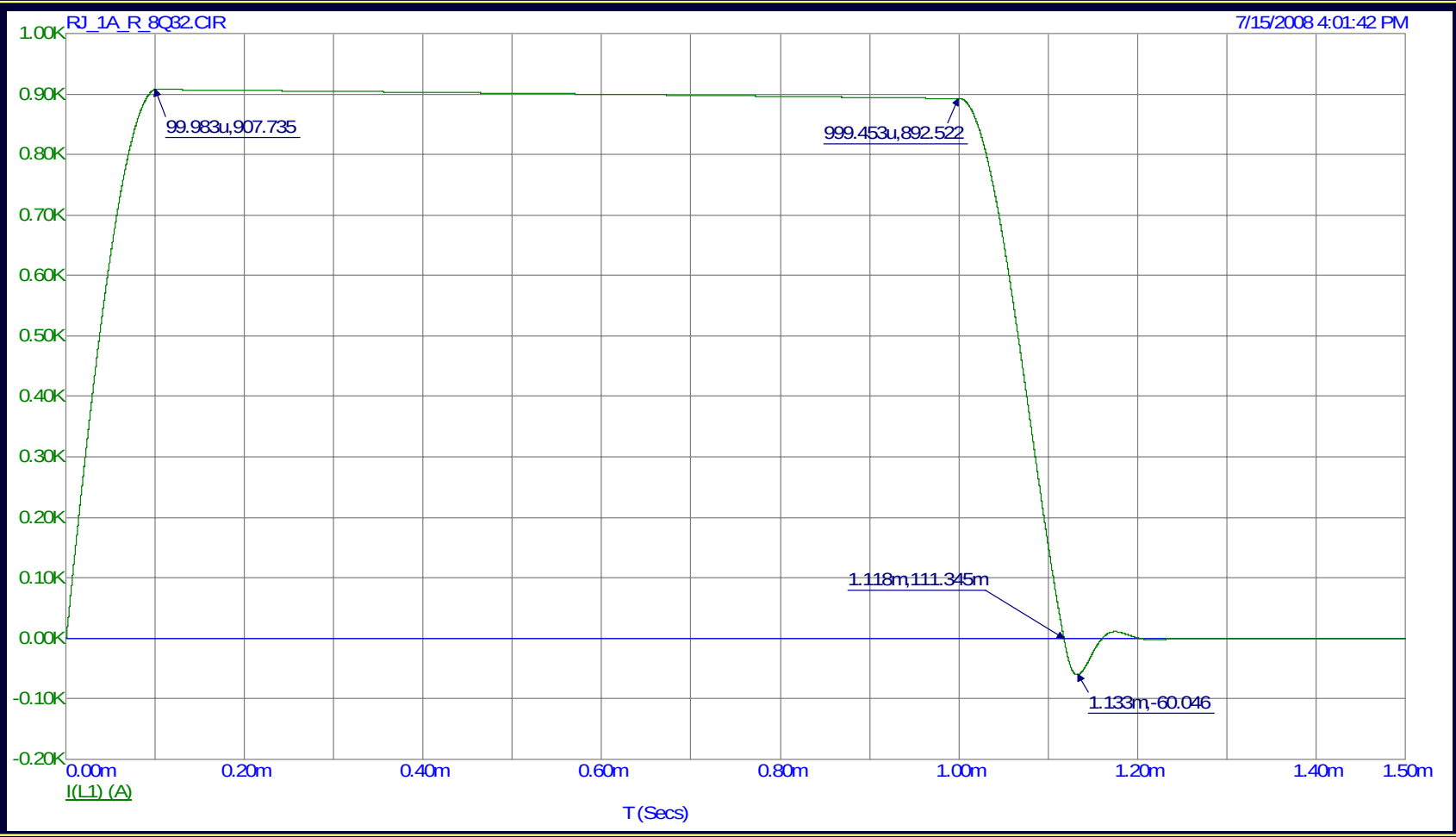
8Q32 with 3 Turn Coil and Coaxial Cable



Simulation


RJ_1A_R_8Q32.CIR
7/15/2008 3:55:08 PM
1.00K
0.60K
0.20K
-0.20K
-0.60K
-1.00K
0.80K
0.40K
0.00K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m

Simulation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7/15/2008 4:01:42 PM
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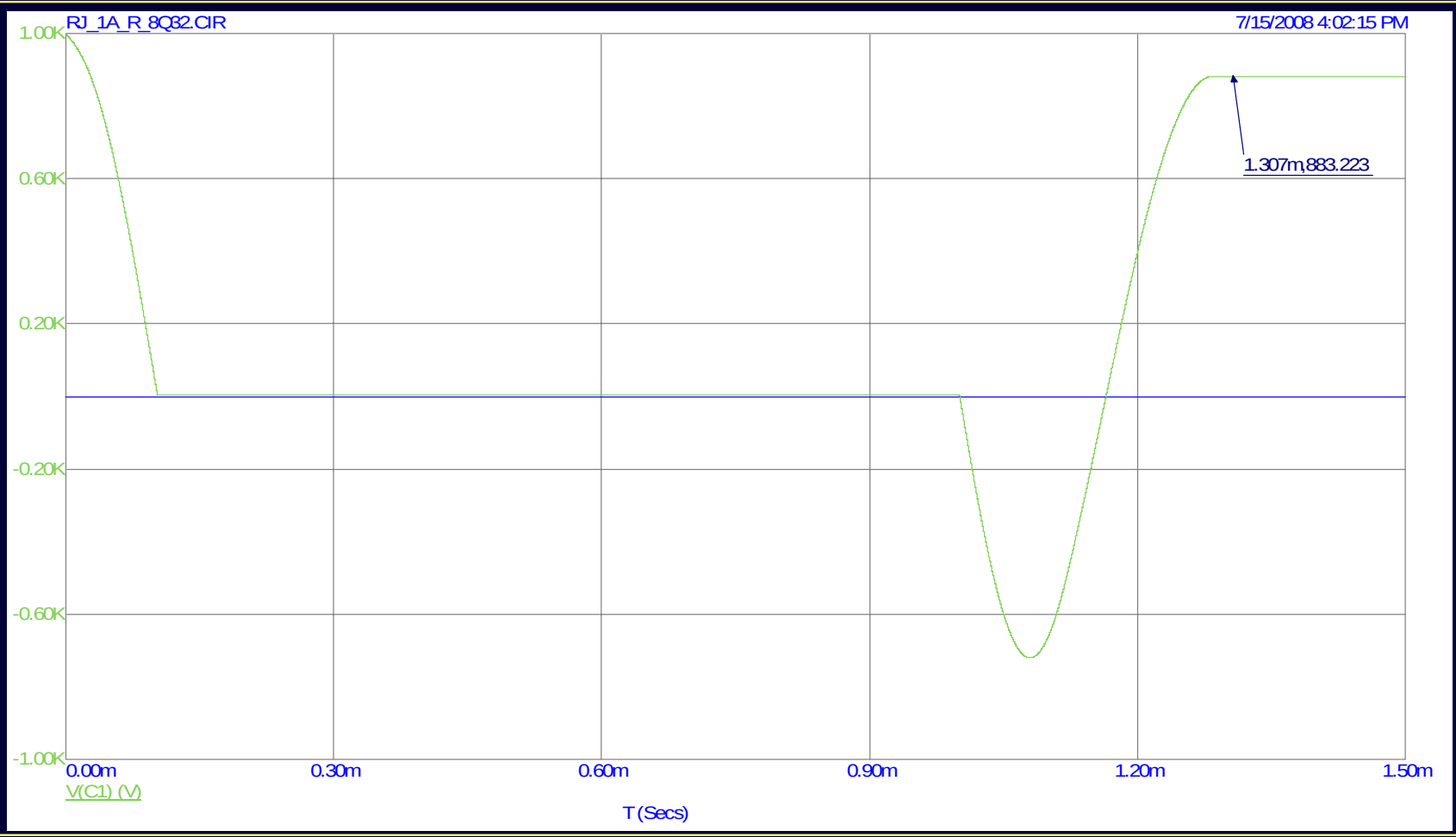
0.90K
0.80K
0.70K
0.60K
0.50K
0.40K
0.30K
0.20K
0.10K
0.00K
-0.10K
-0.20K
99.983u,907.735
999.453u,892.522
1.118m,111.345m
1.133m,-60.046
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
1.20m
1.40m
1.50m
I(L1) (A)
T (Secs)

Simulation


RJ_1A_R_8Q82.CIR
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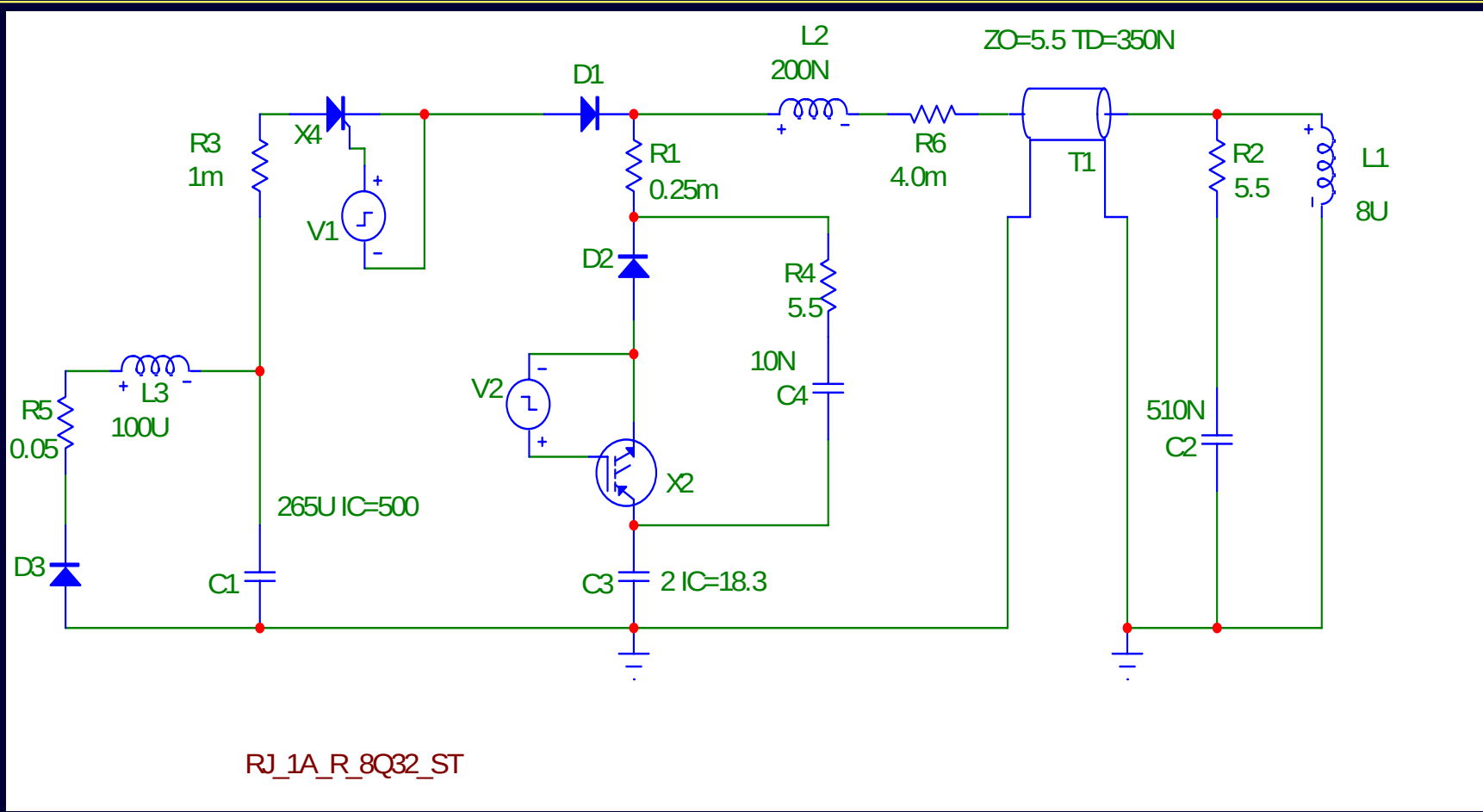
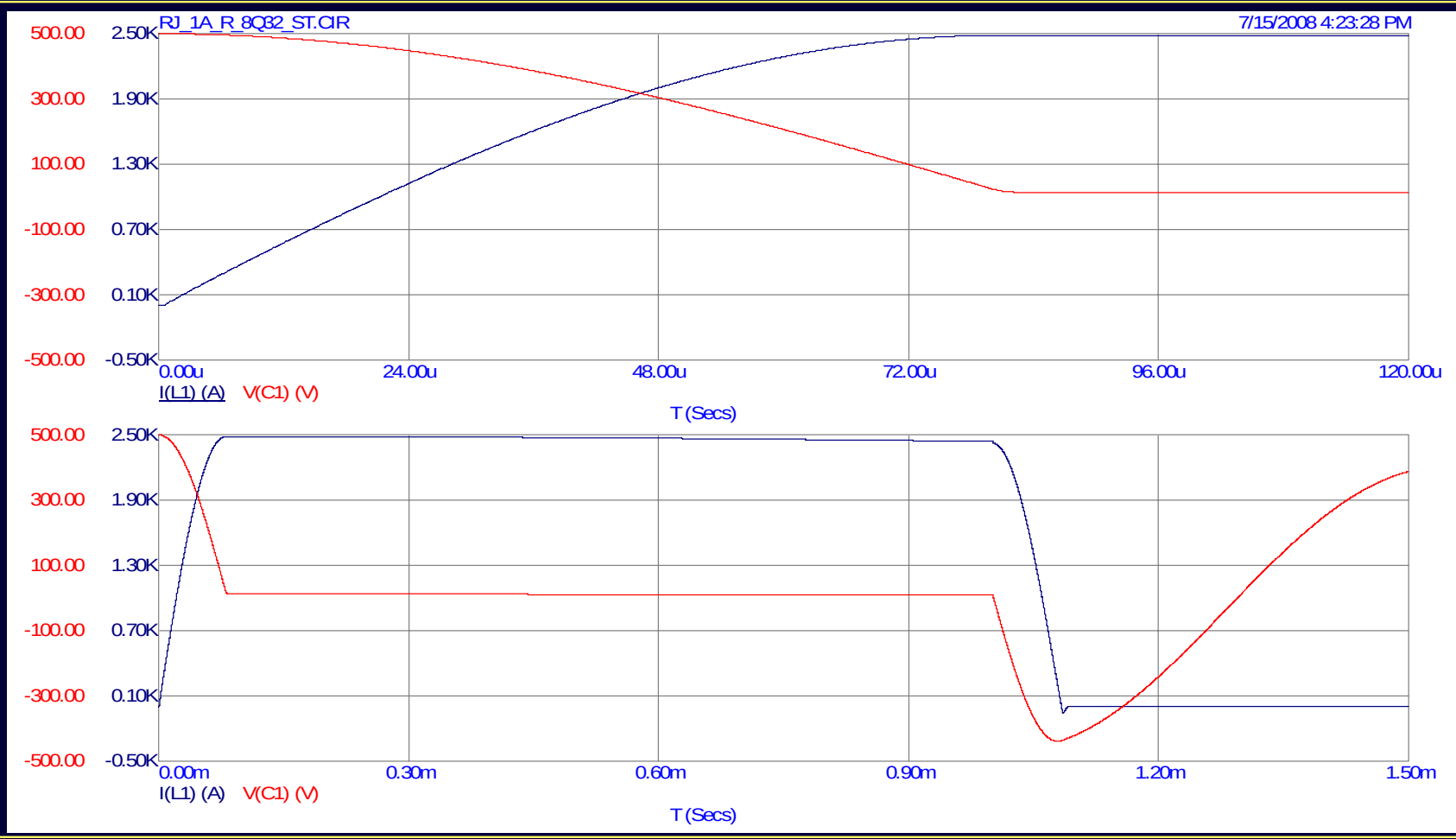
0.60K
0.20K
-0.20K
-0.60K
-1.00K
1.307m,883.223
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
V(C1) (V)
T (Secs)

Proposed Schematic

8Q32 with Single Turn Coil and Coaxial Cable



Simulation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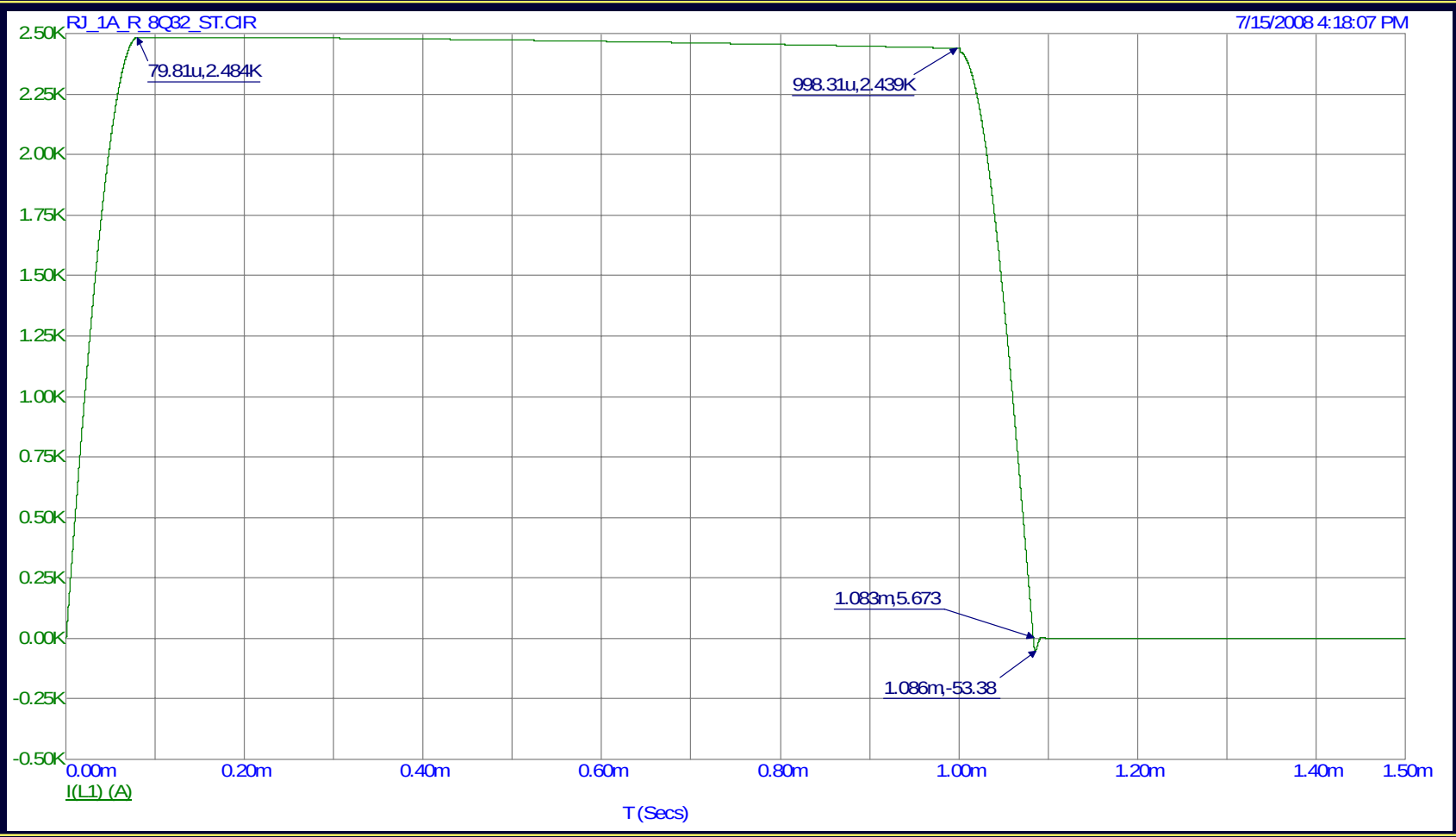
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

Simulation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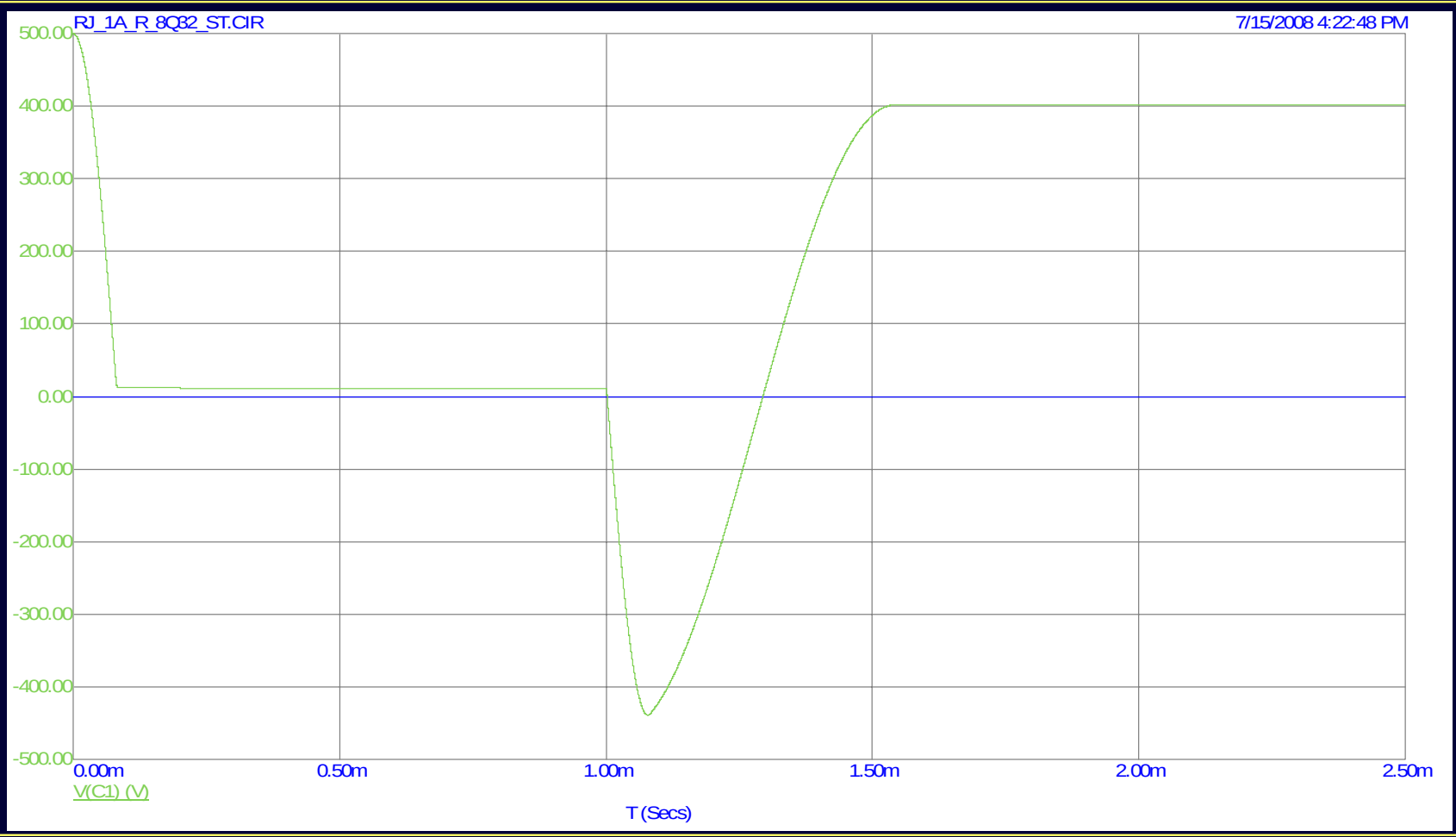
79.81u,2.484K
998.31u,2.439K
1.083m,5.673
1.086m,-53.38
2.50K
2.25K
2.00K
1.75K
1.50K
1.25K
1.00K
0.75K
0.50K
0.25K
0.00K
-0.25K
-0.50K
0.00m
0.20m
0.40m
0.60m
0.80m
1.00m
1.20m
1.40m
1.50m
I(L1) (A)
T (Secs)

Simulation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7/15/2008 4:22:48 PM
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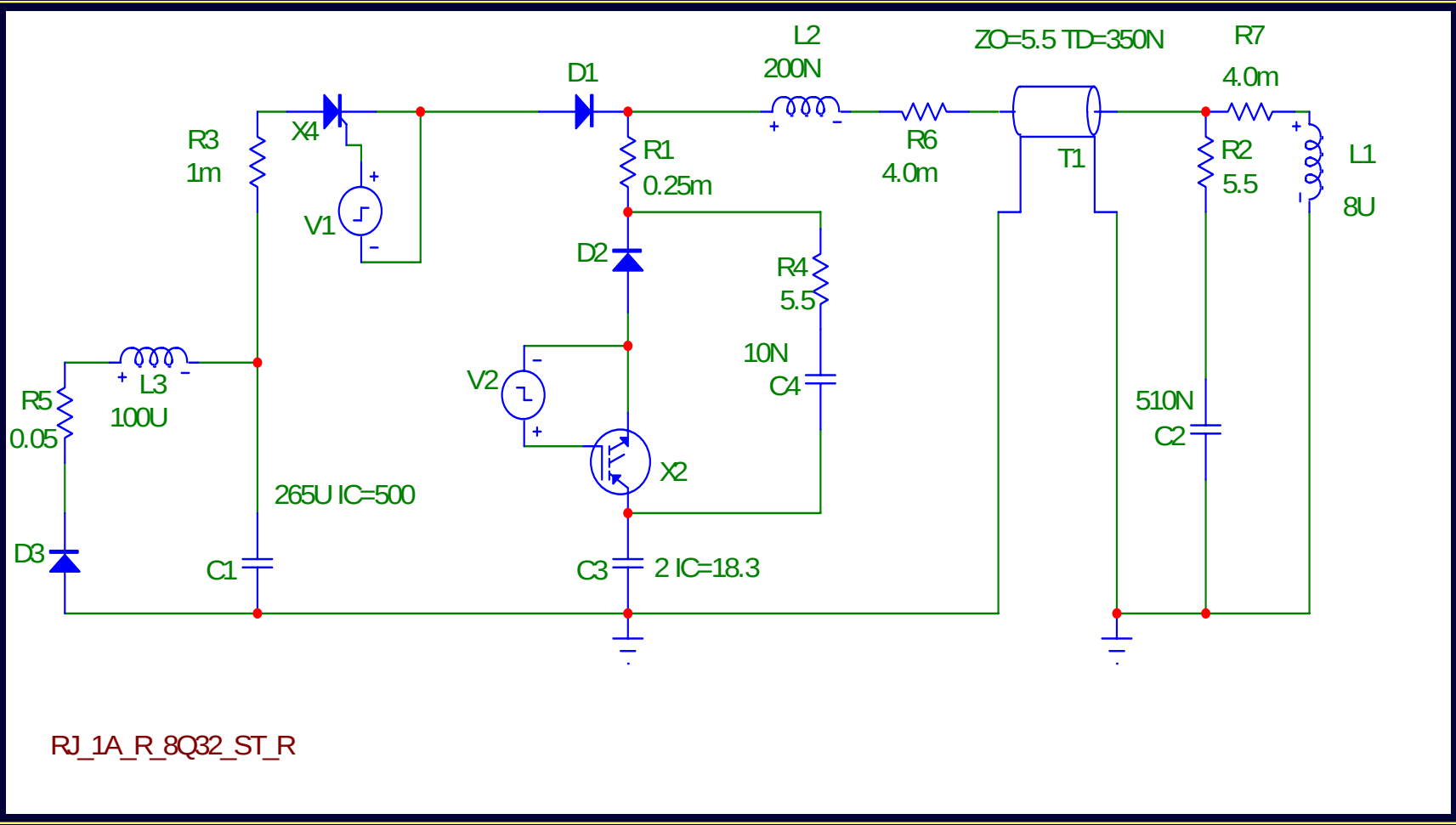
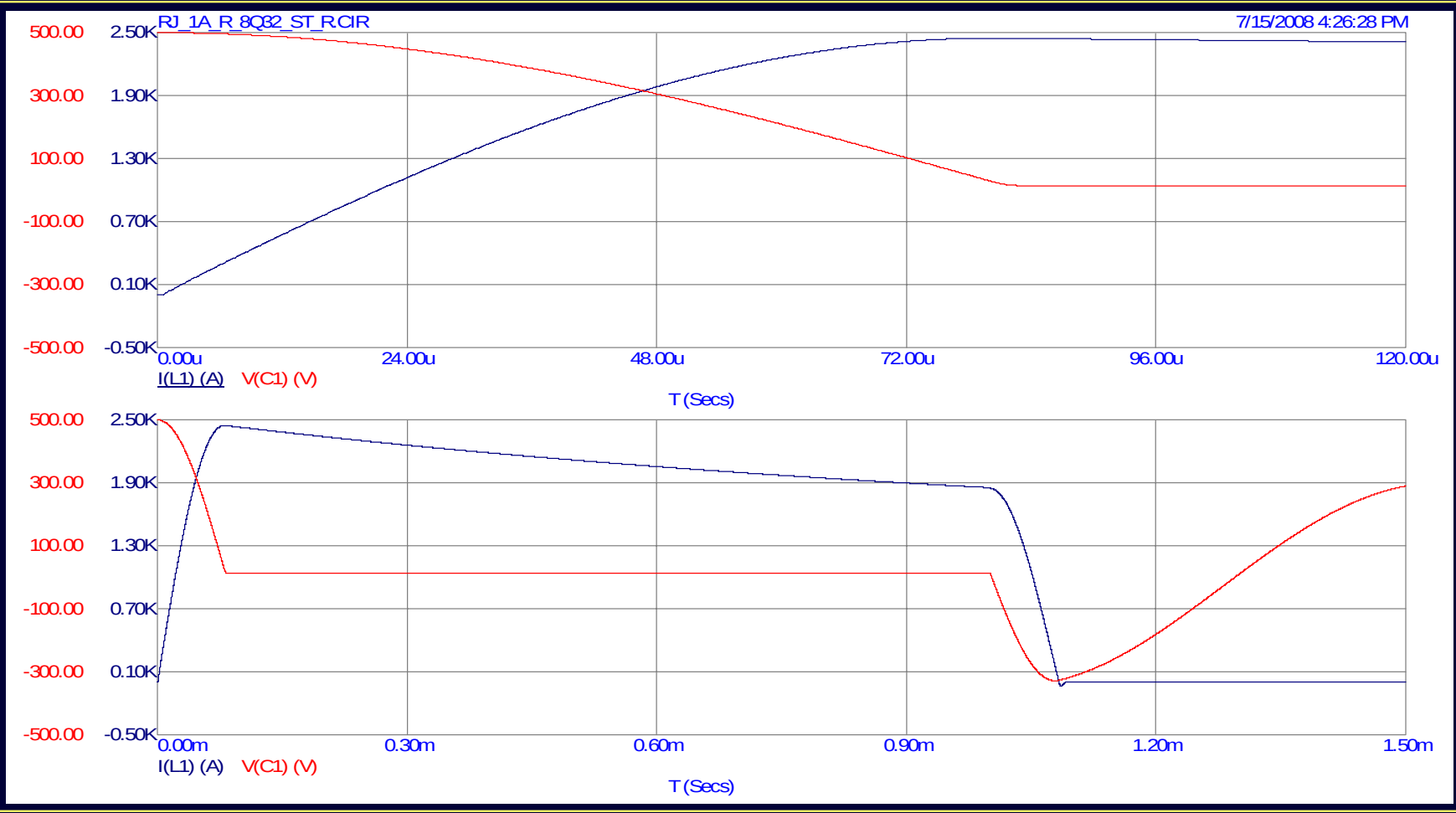
400.00
300.00
200.00
100.00
0.00
-100.00
-200.00
-300.00
-400.00
-500.00
0.00m
0.50m
1.00m
1.50m
2.00m
2.50m
V(C1) (V)
T (Secs)

Resistance Effect



Simulation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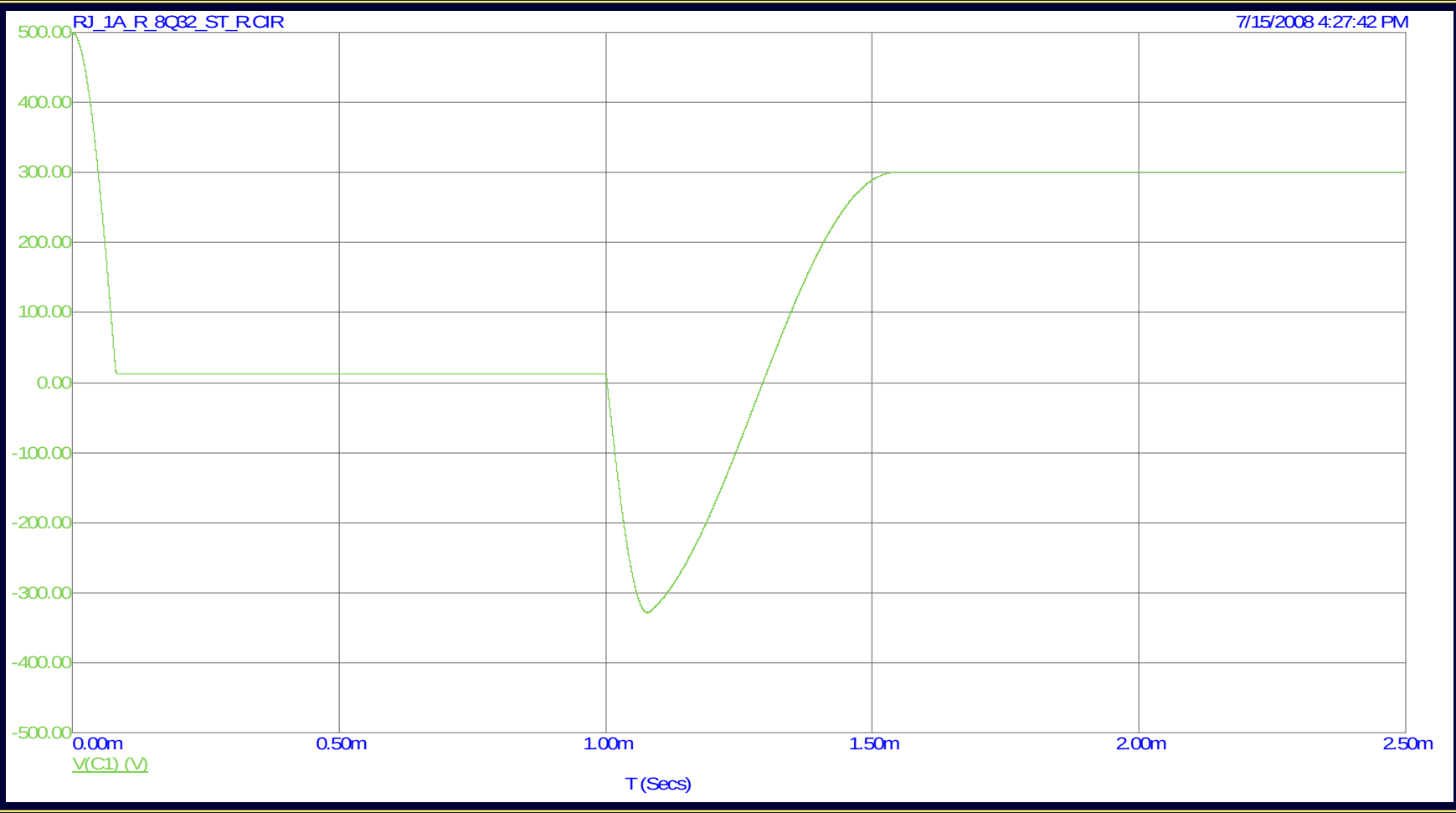
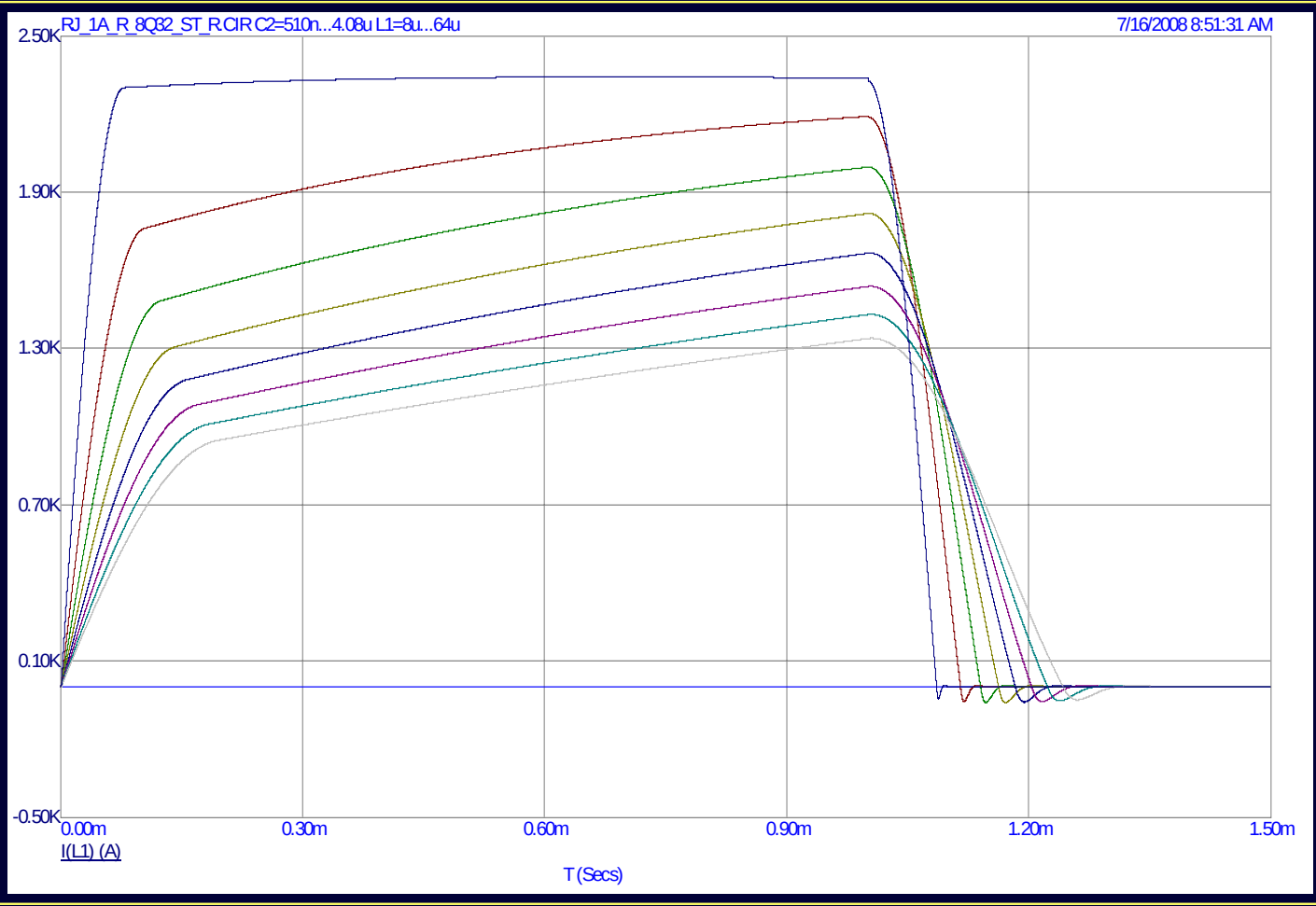
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

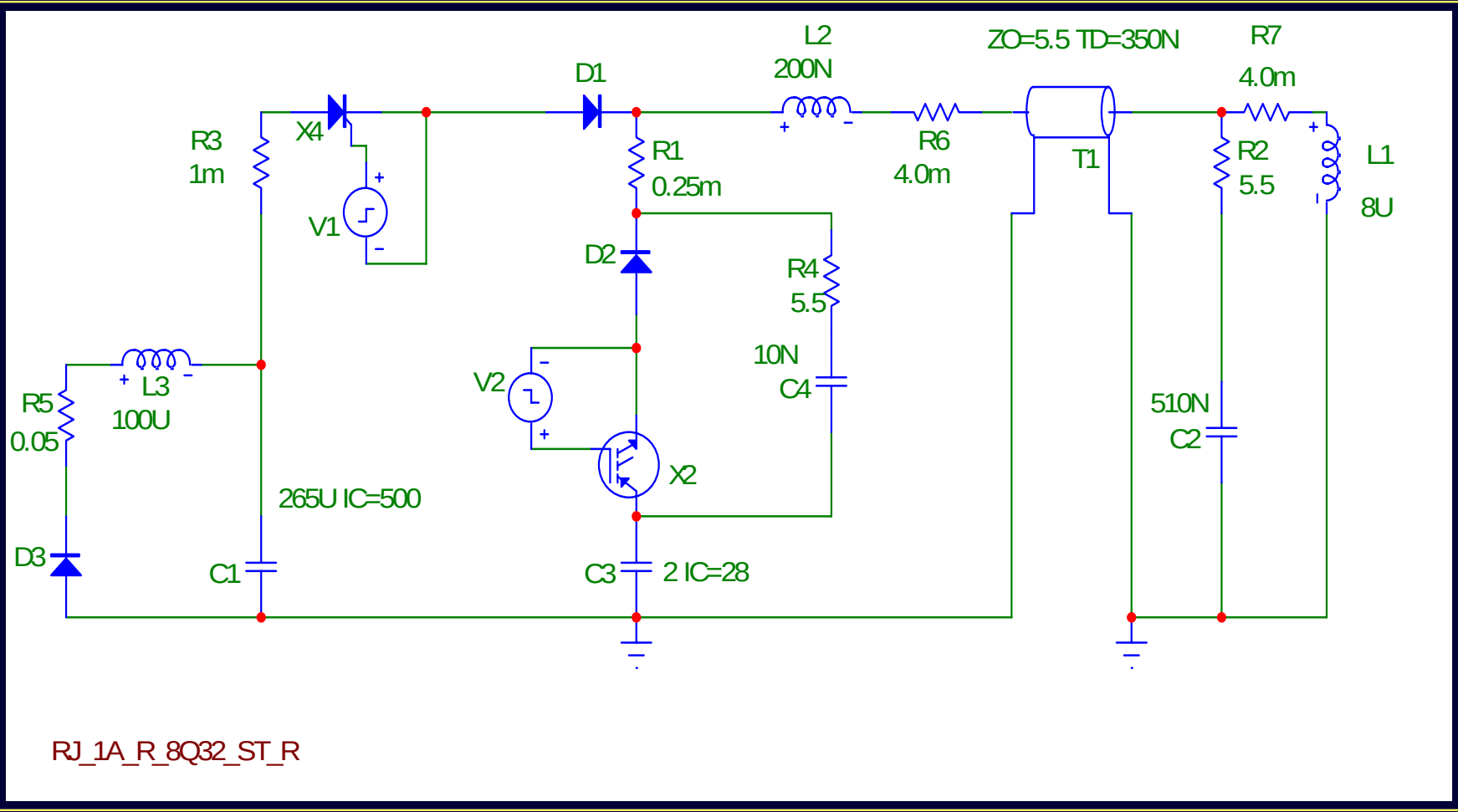
Simulation


RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:27:42 PM
500.00
400.00
300.00
200.00
100.00
0.00
-100.00
-200.00
-300.00
-400.00
-500.00
0.00m
0.50m
1.00m
1.50m
2.00m
2.50m
V(C1) (V)
T (Secs)

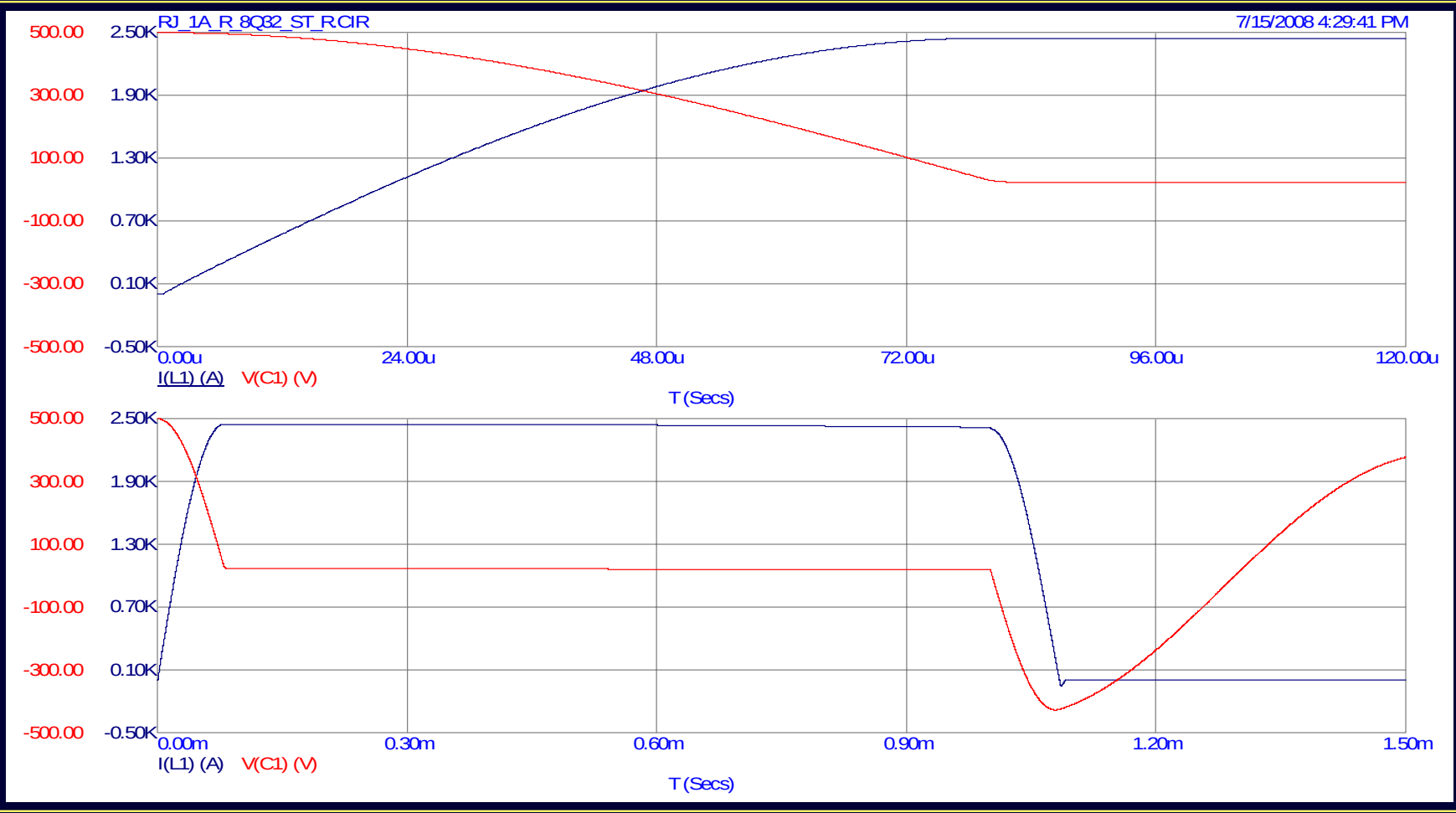
Load Inductance and Pulse Undershoot



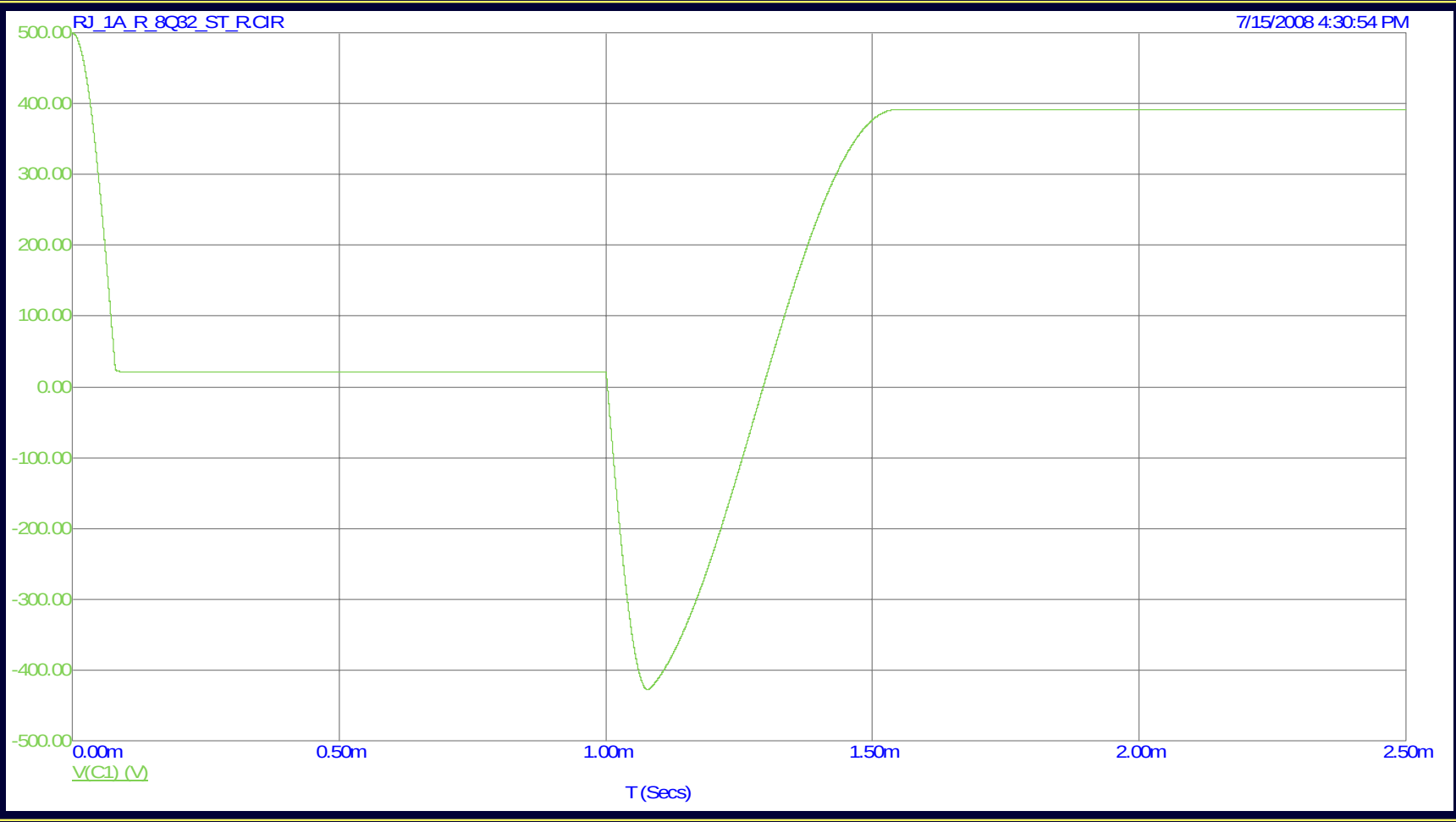
Proposed Schematic



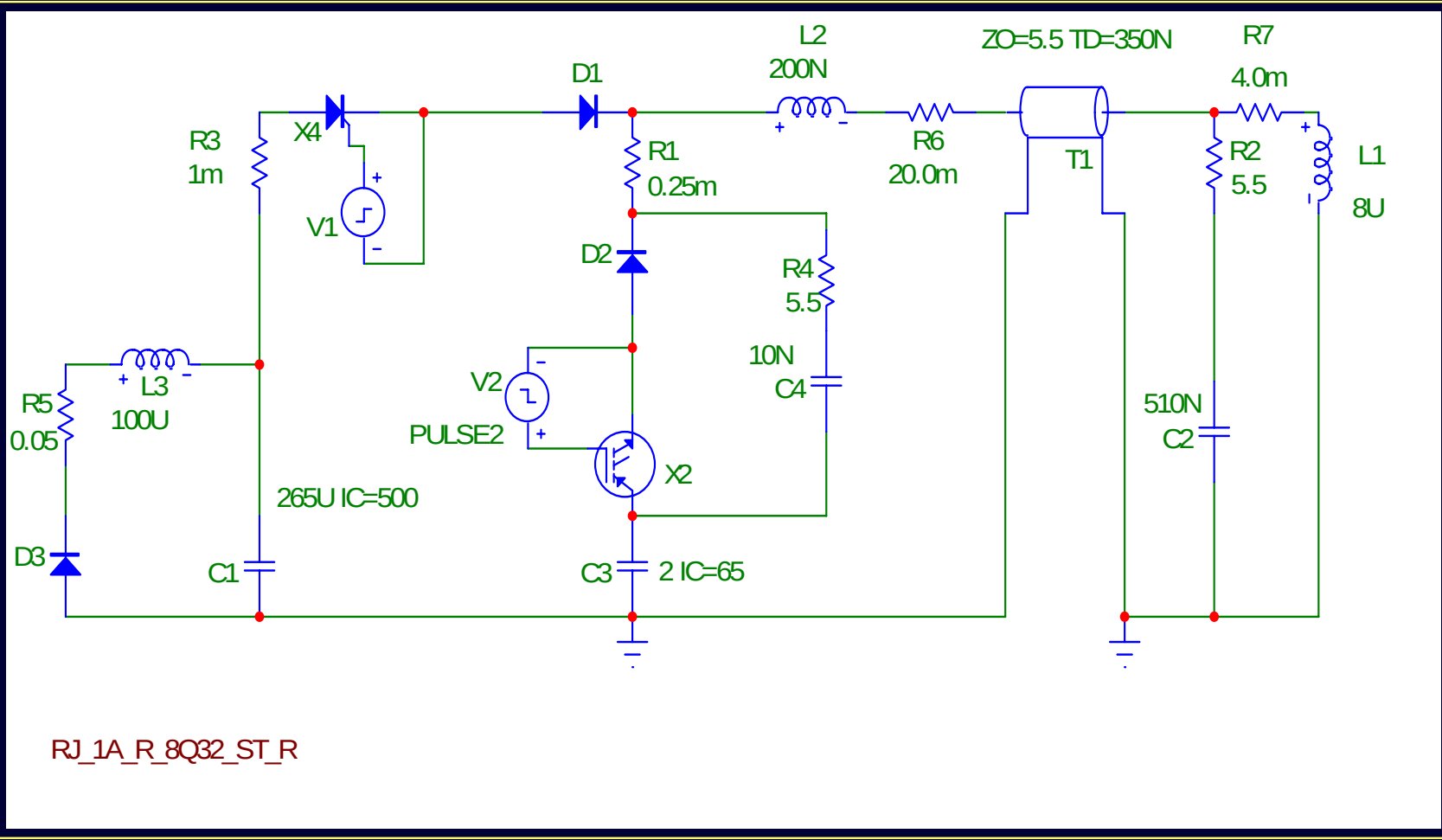
Simulation


RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:29:41 PM
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
V(C1) (V)
T (Secs)

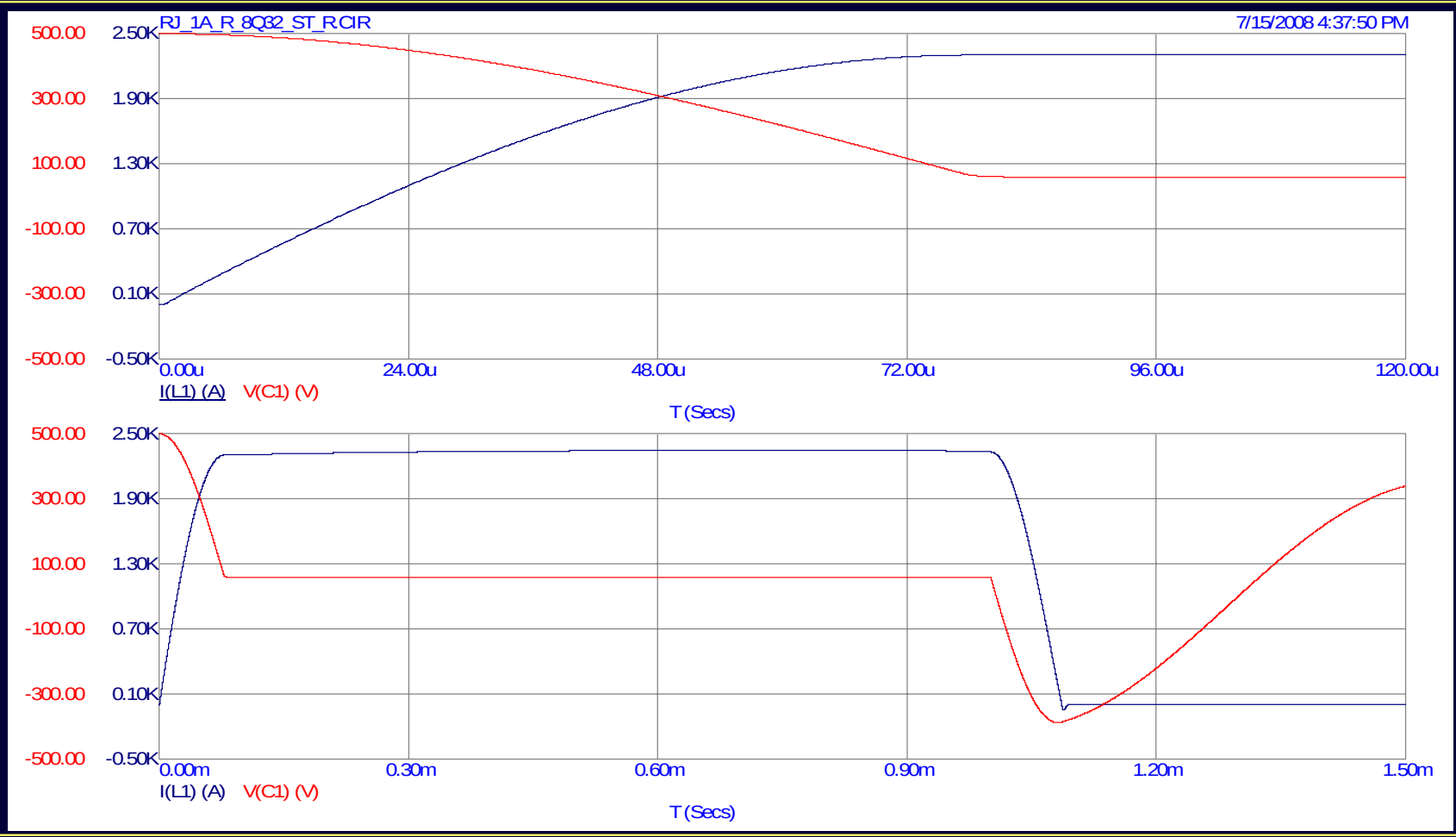
Simulation


RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:30:54 PM
500.00
400.00
300.00
200.00
100.00
0.00
-100.00
-200.00
-300.00
-400.00
-500.00
0.00m
0.50m
1.00m
1.50m
2.00m
2.50m
V(C1) (V)
T (Secs)

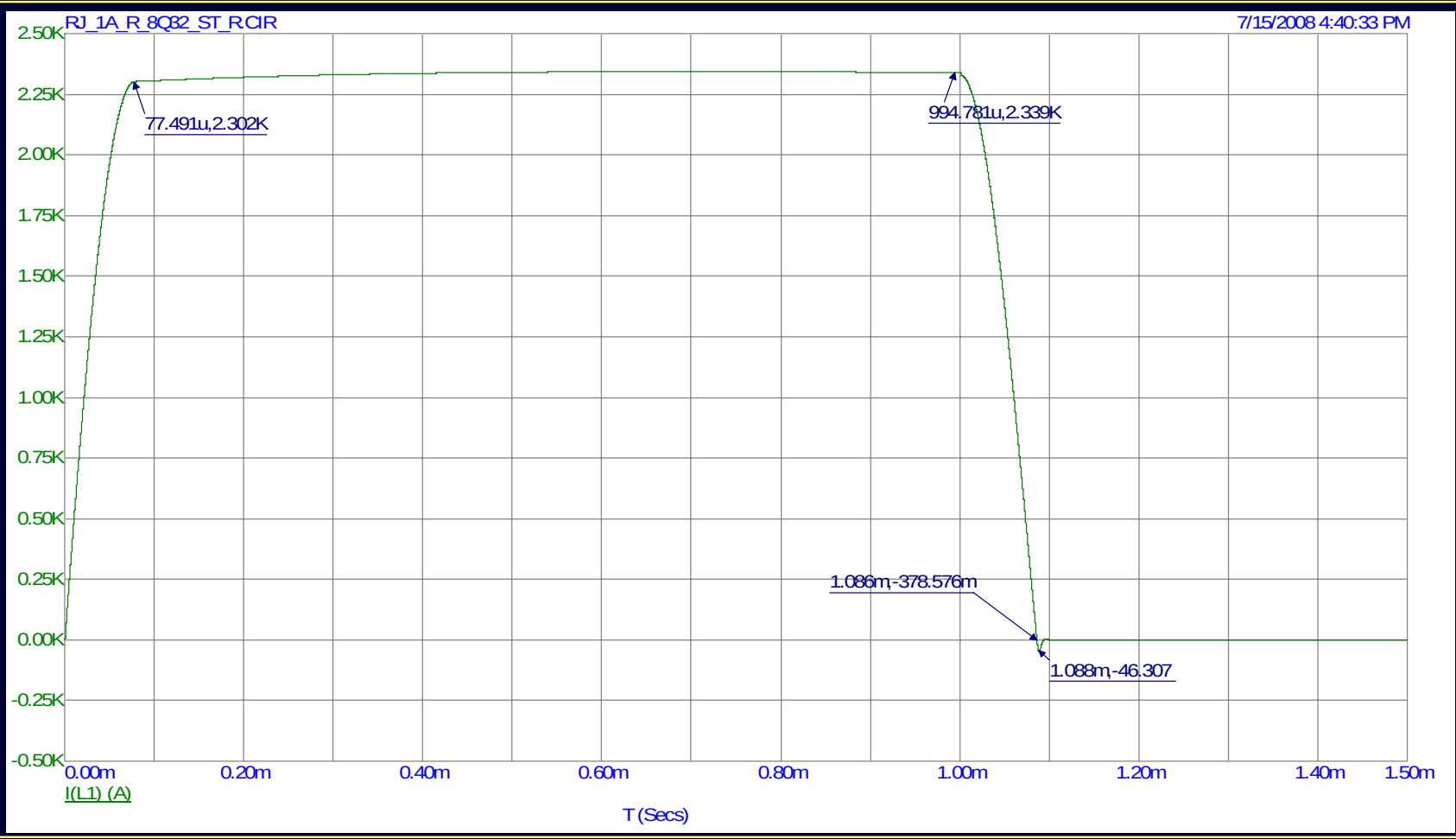
Larger Resistance



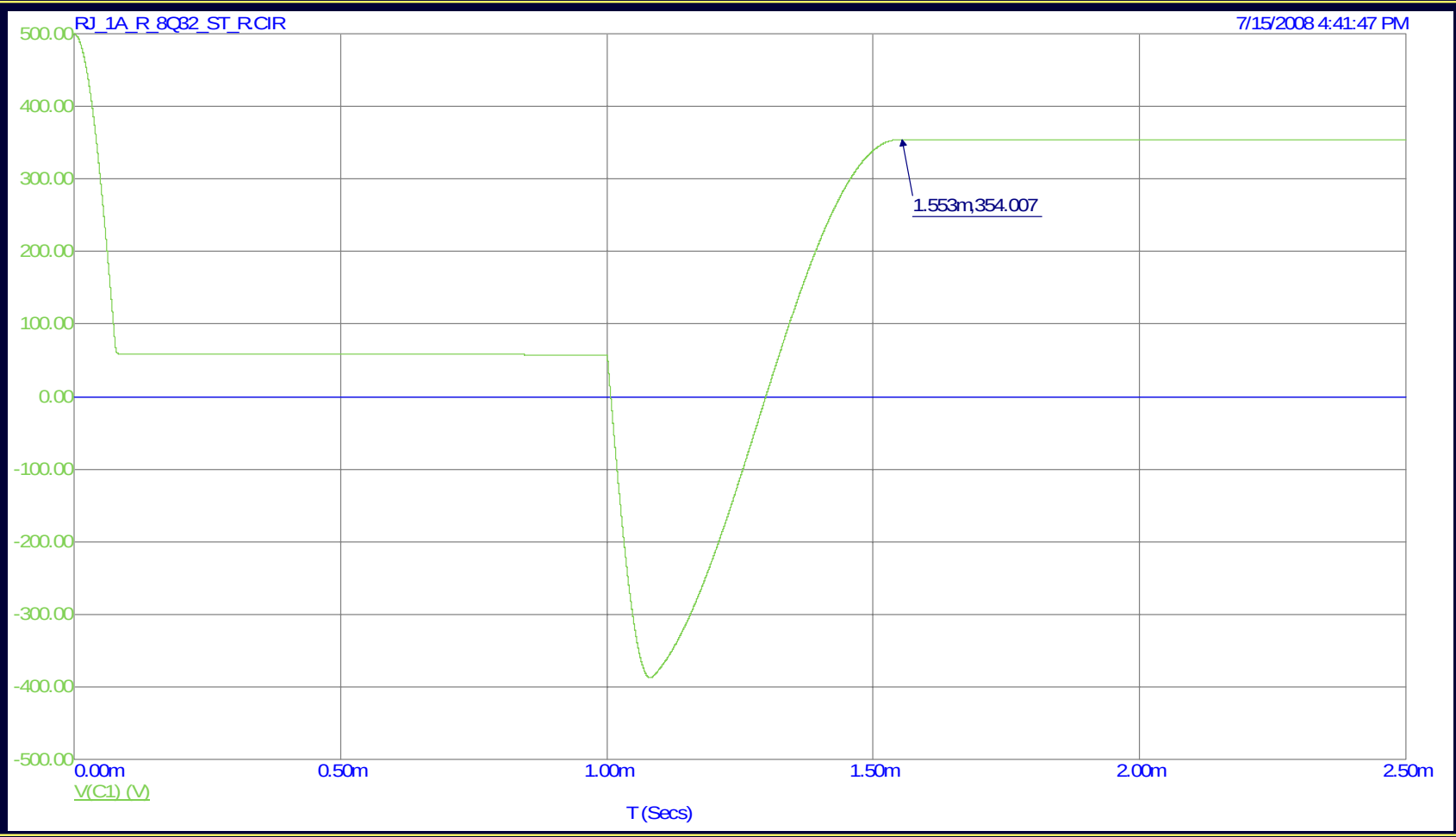
Larger Resistance



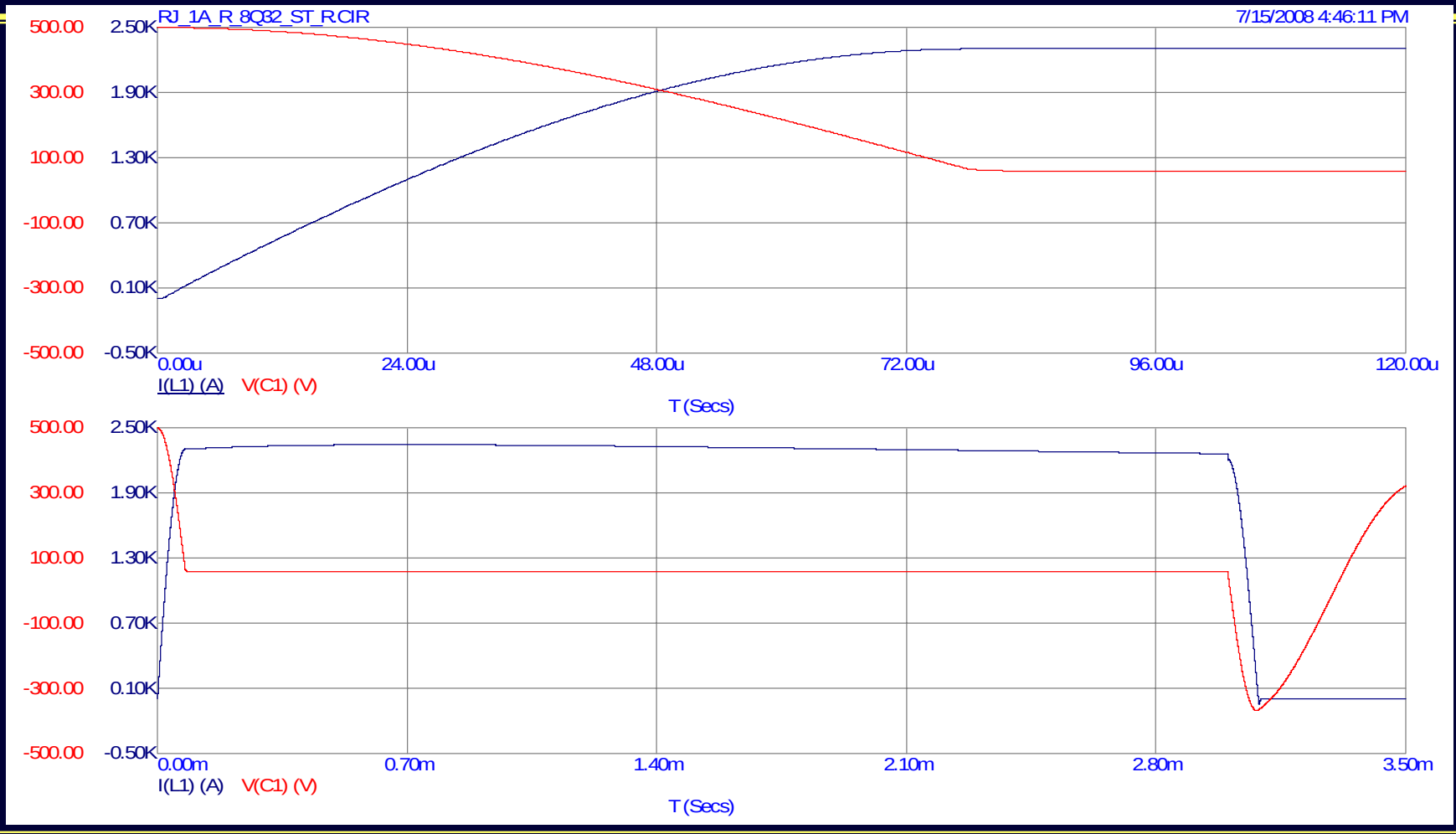
Larger Resistance



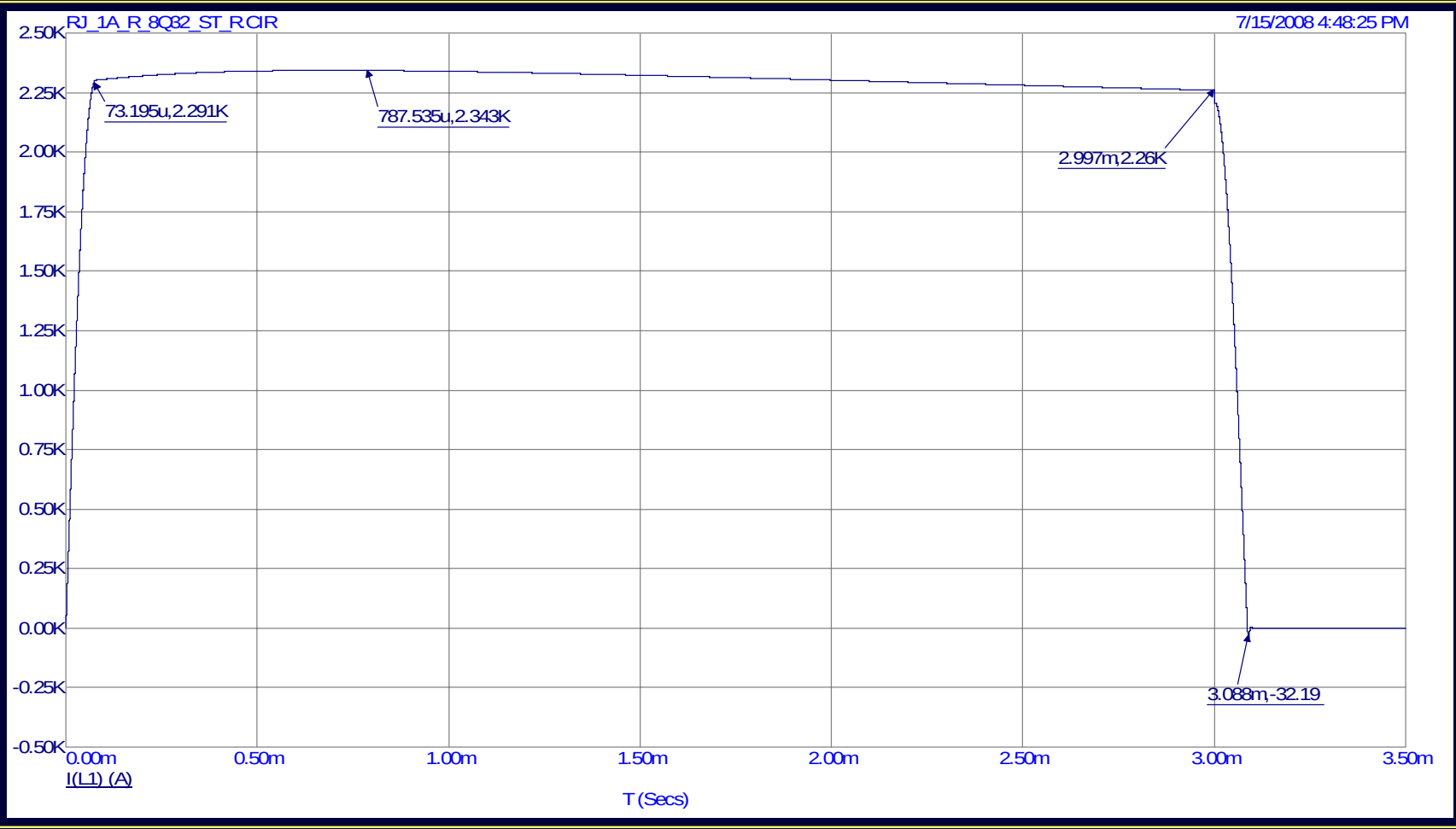
Larger Resistance



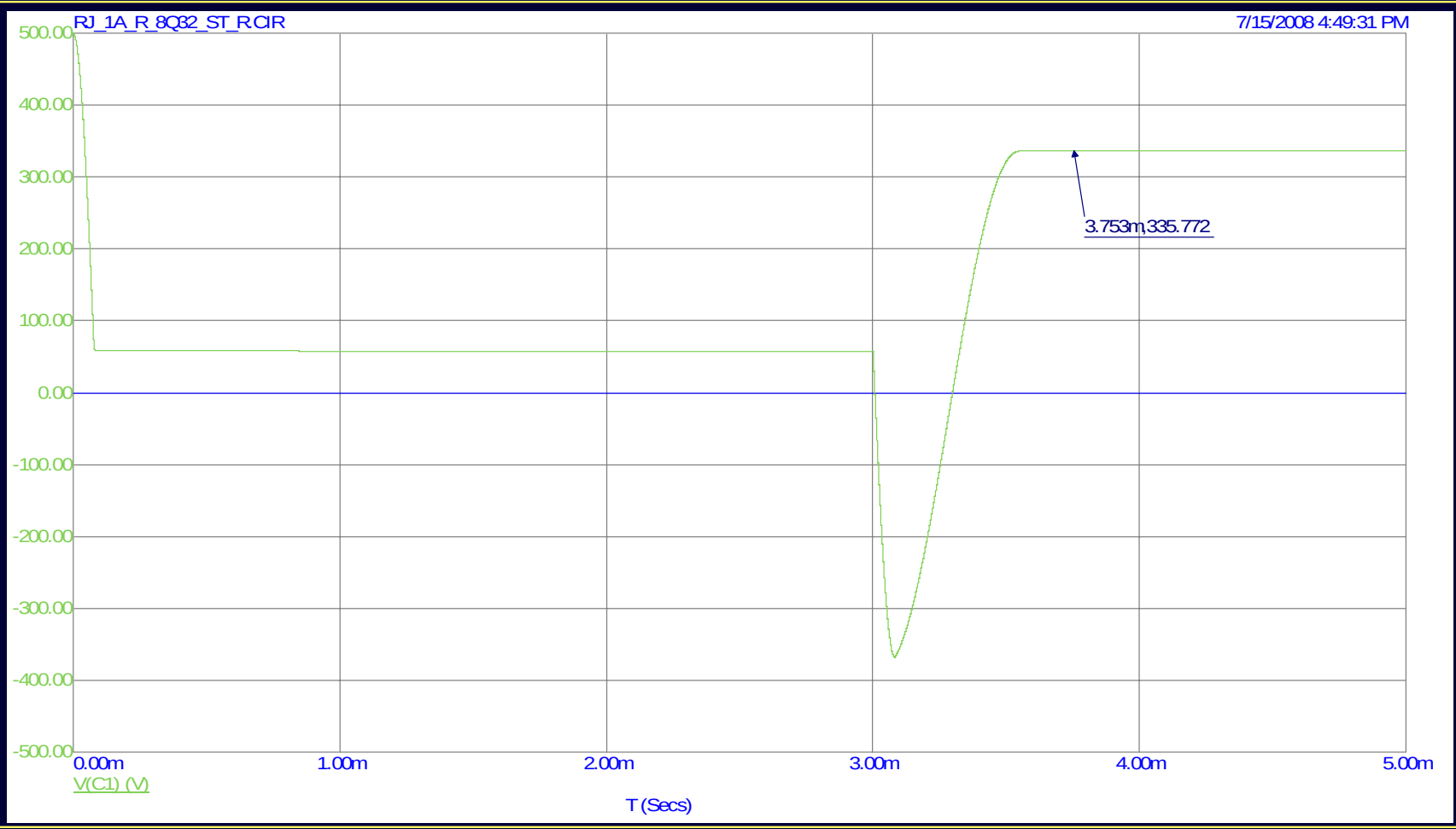
Long Pulse


RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:46:11 PM
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00u
24.00u
48.00u
72.00u
96.00u
120.00u
I(L1) (A)
V(C1) (V)
T (Secs)
500.00
300.00
100.00
-100.00
-300.00
-500.00
2.50K
1.90K
1.30K
0.70K
0.10K
-0.50K
0.00m
0.70m
1.40m
2.10m
2.80m
3.50m
I(L1) (A)
V(C1) (V)
T (Secs)

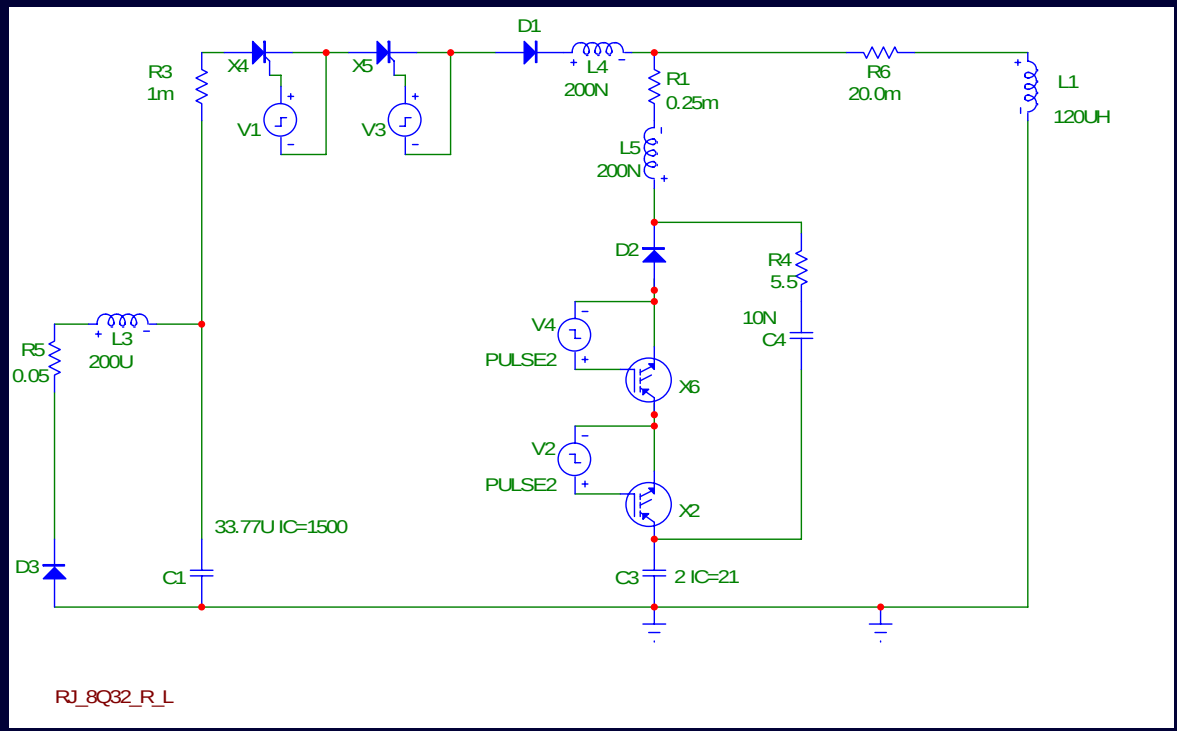
Long Pulse


RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:48:25 PM
73.195u,2.291K
787.535u,2.343K
2.997m,2.26K
3.088m,-32.19
2.50K
2.25K
2.00K
1.75K
1.50K
1.25K
1.00K
0.75K
0.50K
0.25K
0.00K
-0.25K
-0.50K
0.00m
0.50m
1.00m
1.50m
2.00m
2.50m
3.00m
3.50m
I(L1) (A)
T (Secs)

Long Pulse

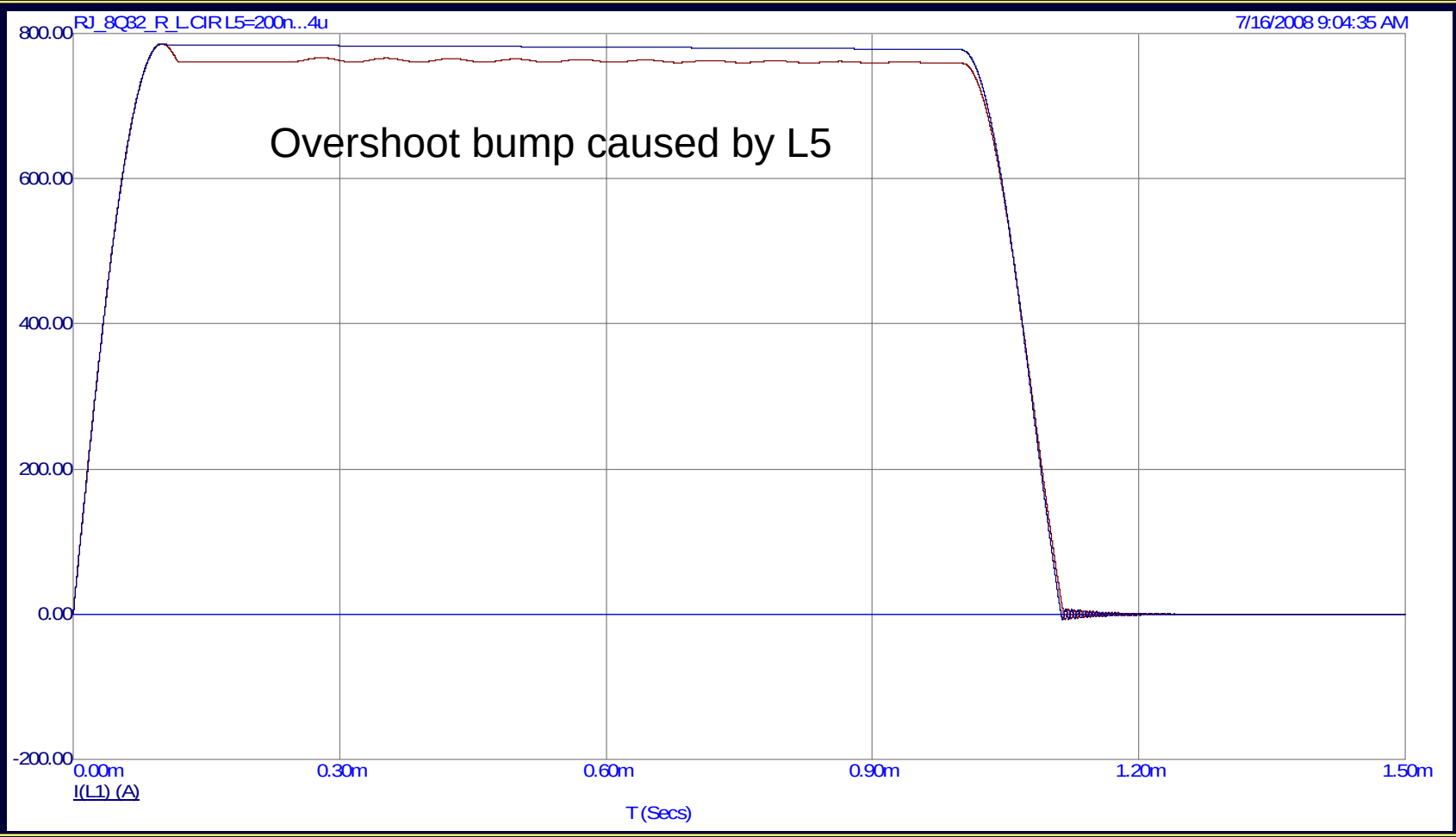

RJ_1A_R_8Q32_ST_R.CIR
7/15/2008 4:49:31 PM
500.00
400.00
300.00
200.00
100.00
0.00
-100.00
-200.00
-300.00
-400.00
-500.00
3.753m,335.772
0.00m
1.00m
2.00m
3.00m
4.00m
5.00m
V(C1) (V)
T (Secs)

Parasitic Inductance Effect

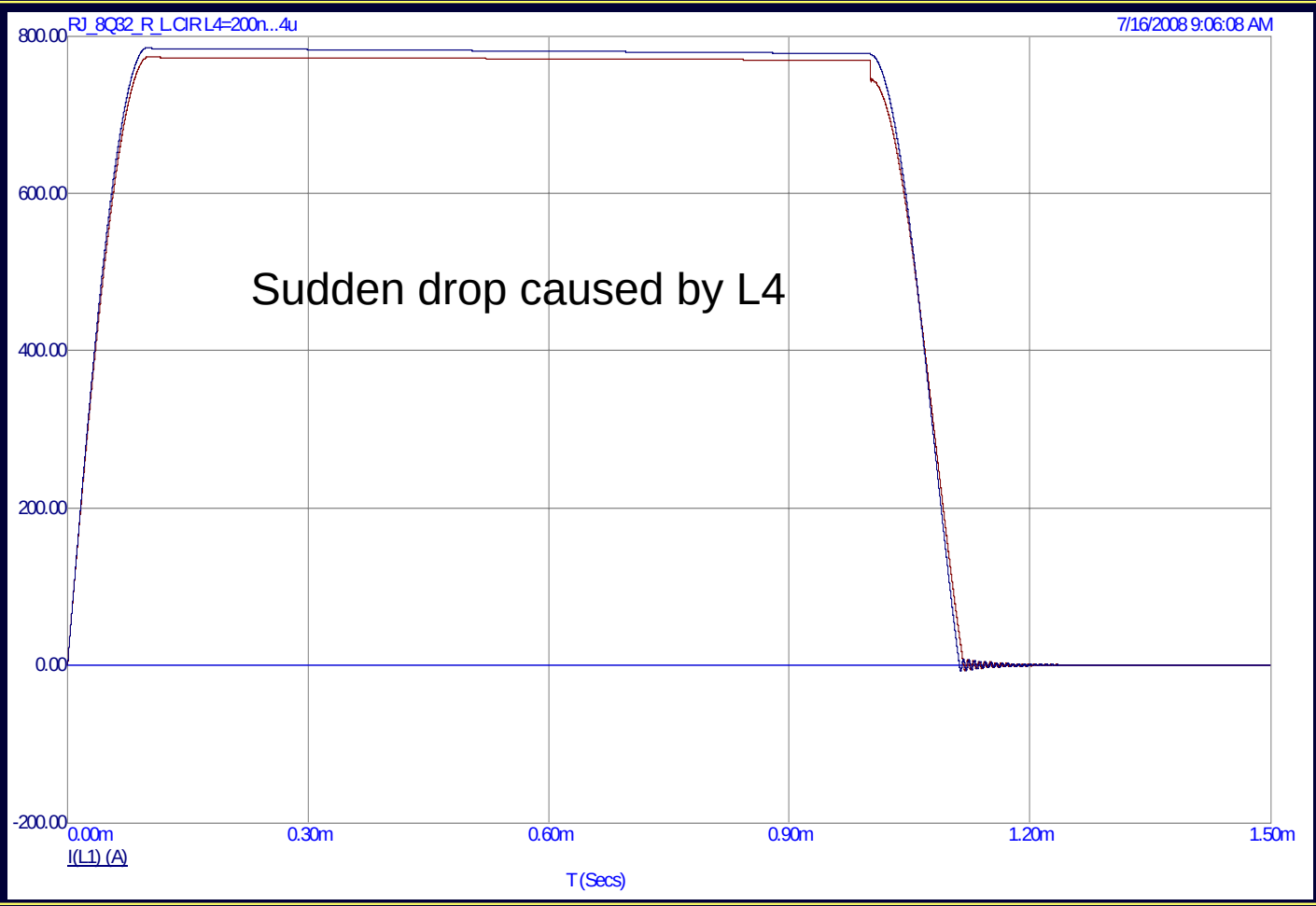


Parasitic Inductance Effect

Simulation


RJ_8Q82_R_L CIR L5=200n...4u
7/16/2008 9:04:35 AM
Overshoot bump caused by L5
800.00
600.00
400.00
200.00
0.00
-200.00
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
T (Secs)

Simulation


RJ_8Q32_R_L.CIR L4=200n...4u
7/16/2008 9:06:08 AM
800.00
600.00
400.00
200.00
0.00
-200.00
Sudden drop caused by L4
0.00m
0.30m
0.60m
0.90m
1.20m
1.50m
I(L1) (A)
T (Secs)

Cable Inductance

- Cable inductance can be reduced by using Coaxial Cables
- Suggested cables
  - RG213
  - DSI 2241
  - DSI 2139
  - DSI 2255
- Coaxial cables have lower cost

Pulse Flat-top Flatness

- 10% seems to be reasonable to achieve

Pulse Rise/Fall Edge Symmetry

- Slight difference has been observed
- Fall time is ~10% longer than rise time
- Further investigation will be conducted

Pulse Overshoot

- Caused by parasitic inductance
- Lower loop inductance can reduce pulse overshoot
- → Construction and Layout with low inductance

Pulse Undershoot

- Might be caused by load inductance
- Higher the load inductance, bigger the pulse undershoot?
- Lower inductance preferred
- Further investigation

Resistance Effect

- Slight impact on peak current amplitude
- Larger impact on low voltage capacitor charging voltage
- Resistive heating
- Construction and layout with low resistive material and structure
- Components with low “ON” resistance

Conclusion

- Coaxial cable will lower total inductance
- Coaxial cable will lower main bank voltage
- Single turn coil will lower load inductance
  - With coaxial cable connection the main bank voltage will be lowered to within voltage rating of existing fast bump capacitor
  - Smaller undershoot
- Cooling method has to be investigated

Pulse Waveform Specifications Option 2 – Bipolar Triangles